

Designing CMOS/Molecular Memories while Considering Device Parameter Variations

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In recent years many advances have been made in the development of molecular scale devices. Experimental data shows that these devices have potential for use in both memory and logic. This paper describes the challenges faced in building crossbar array based molecular memory, and develops a methodology to optimize molecular scale architectures based on experimental device data taken at room temperature. In particular, we discuss reading and writing such memory using CMOS and compiling a solution for easily reading device conductivity states (typically characterized by very small currents). Additionally, a metric is derived to determine the voltages for writing to the crossbar array. Simulation results, incorporating experimental device data, are presented using Cadence Spectre.

Categories and Subject Descriptors: B.7.1 [Integrated Circuits]: Types and Design Styles—*Advanced technologies, Memory technologies, VLSI*

General Terms: Design, Experimentation

1. INTRODUCTION

The infant field of molecular nanoelectronics is often defined as including any technology whose device feature sizes are on the scale of single molecules [Goldhaber-Gordon et al. 1997]. One intriguing technology family within this field consists of devices based on self-assembled monolayers (SAM) of molecules sandwiched between two conducting terminals. Experiments have shown how such devices could be fabricated with useful properties such as rectification, hysteresis and negative differential resistance [Reed 1999; Collier et al. 2000; Majumdar et al. 2005; Donhauser et al. 2001]. Researchers are also making great strides towards integrating these devices into novel electronic circuits [Luo et al. 2002]. As molecular electronics matures to the point of fabricating molecular memory

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and logic, circuit level considerations must be assessed in order to expedite development. Similarly, approaching design from the circuits level of abstraction allows a connection between what is theoretically possible from an architectural point of view and what can actually be achieved in terms of fabrication.

A common structure in which SAM-based devices have been considered and fabricated to date is known as the crossbar array, which consists of two sets of parallel wires crossing perpendicularly [Ziegler and Stan 2002]. Between each wire crossing exists a SAM of molecules such that the overall circuit is an array of two-terminal molecular devices. The device explored here is a SAM-based molecular device that shows electrical switching with memory (hysteresis). The molecule this device is based on is referred to here as the “nitro” molecule and it exhibits this hysteretic switching behavior. If the devices are programmable, as are the ones considered in this paper, then the resulting circuit can be used to implement either memory or programmable logic. As can be seen in Fig. 1, a crossbar array is a regular structure which eases fabrication, a primary motivation for using such circuits. Another motivating factor for developing such memories is the fact that most results show these devices to be non-volatile, placing the technology in a category with Flash RAM and magnetic memory. Some in the field, including H-P Labs and Caltech, have already accomplished the fabrication of molecular crossbar arrays for use as memory and are continuing toward the development of larger, denser arrays [Luo et al. 2002; Chen et al. 2000]. As such circuits scale to accommodate greater memory and logic requirements, circuit level issues, which may limit scaling, must be addressed.

The focus of this work is to really delve into the circuit details of developing memory based on actual fabricated devices. Some recent work performed by DeHon et al. begins to examine the circuit level challenges facing molecular memory [DeHon et al. 2005]. Here they perform theoretical calculations for power, delay, and area assuming ideal diode like devices for their memory. This work goes one step further by performing circuit simulations using actual devices modeled for use in Cadence Spectre. Additionally, this work implements all of the memory control circuitry, i.e. row and column decoders, in the CMOS layer, where previous works stress implementing this circuitry in the nano layer [DeHon et al. 2005]. In [Strukov and Likharev 2005], the authors discuss a way to combine CMOS level control circuitry with crossbar array based memory, showing the feasibility of combining these two different circuit elements on one substrate.

In this paper, we discuss reading and writing the crossbar array based memory from CMOS, compiling a solution for reading very small currents through these molecular devices, and a metric to calculate voltages for writing to the crossbar array. We discuss memory size limitations based on device rectification and on/off current ratios. Proposed is a design approach for minimizing the effects of these limitations that touches on both circuit and device level improvements. Additionally we discuss device variations, in particular the variations in device toggle voltage and device conductivity, and how they impact the overall circuit performance. We estimate the maximum allowable conductivity and toggle voltage variations in order to maintain memory functionality. Using Cadence Spectre, we present room temperature simulation results for reading and writing the crossbar array. All models for our “nitro” molecule are compiled using the universal device model (UDM) [Rose et al. 2004] developed at the University of Virginia.

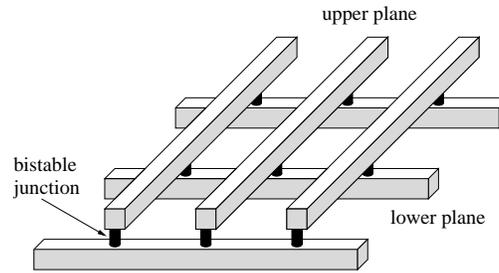


Fig. 1. The crossbar paradigm consists of perpendicular sets of parallel wires with bistable junctions at each wire crossing.

2. MOLECULAR ELECTRONIC DEVICES AND CIRCUITS

2.1 Experimental Results: Electrical Behavior of a Molecular Device

In the area of molecular electronics, researchers are exploring different combinations of organic molecules with varying electrical behaviors and molecular structures. We have designed and fabricated such a device structure and used it to test an oligo(phenylene ethynylene) molecule with a nitro sidegroup (Fig. 2a), a molecule that has shown potential for use in logic as well as memory. An illustration of this test structure is shown in Fig. 2b and is called the nanowell device [Majumdar et al. 2006; Gergel et al. 2005]. This device consists of a “well” with a diameter of 10-50 nm, a depth of 100nm, silicon dioxide sides, and a gold bottom.

The starting substrate for the nanowell is a silicon wafer covered with silicon dioxide, patterned with gold and a top layer of silicon dioxide 100nm thick. A focused ion beam (FIB) is used to mill the well through the top silicon dioxide to expose the bottom Au. This structure is then placed into a solution of the self-assembling molecules, each containing a sulfur endgroup giving it a chemical affinity for gold. These molecules assemble in an upright position on the gold surface, forming only a single monolayer of molecules. Once assembled, a top contact is made by evaporating titanium and then gold on the molecules in the device. This results in the completed nanowell device illustrated in Fig. 2b. The top and bottom contacts were probed to obtain the current vs. voltage (I-V) characteristics of the devices.

Different groups have observed varying electrical characteristics from this molecule including an asymmetric hysteretic behavior [Reed et al. 2001; Li et al. 2003; Kratochvilova et al. 2002; Fan et al. 2002; Donhauser et al. 2001; Lewis et al. 2004]. This behavior can be seen in the experimental room temperature I-V results of Fig. 3. One can observe in Scan 1 that at -2.3 V, the current switches from a high conductivity state to a low conductivity state and then continues on a lower conductivity path. We labeled -2.3 V in Fig. 3 as $-V_{toggle}$ to signify that this is the switching point, or toggle voltage. In Scan 2, the voltage is again applied from 0 to -3 V and the current remains in the low conductivity state as expected. In Scan 3, we apply a voltage bias from 0 V to +3 V, and one can observe a change in the slope of the I-V curve around +2.5 V on the forward bias. This sudden increase in current marks the transition from the low conductivity state to the high conductivity state; we call this the forward bias toggle voltage ($+V_{toggle}$). Scan 4 shows that as the forward bias is applied from 0 V to +3 V again, the device remains in the high conductivity state [Gergel et al. 2005].

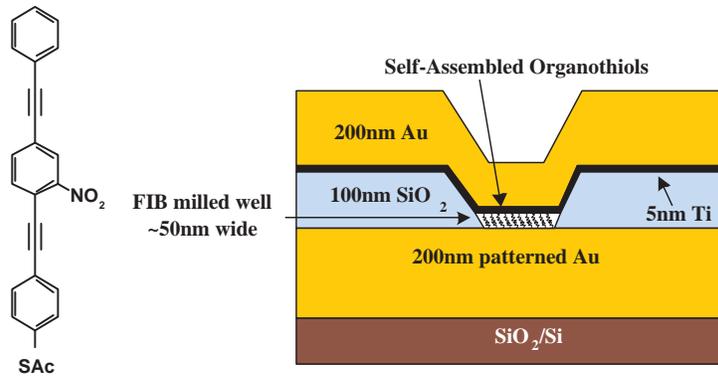


Fig. 2. (a) The nitro-OPE molecule, which had its acetate moiety removed with acid during the assembly process of the free thiol. (b) A cross-section of the nanowell device.

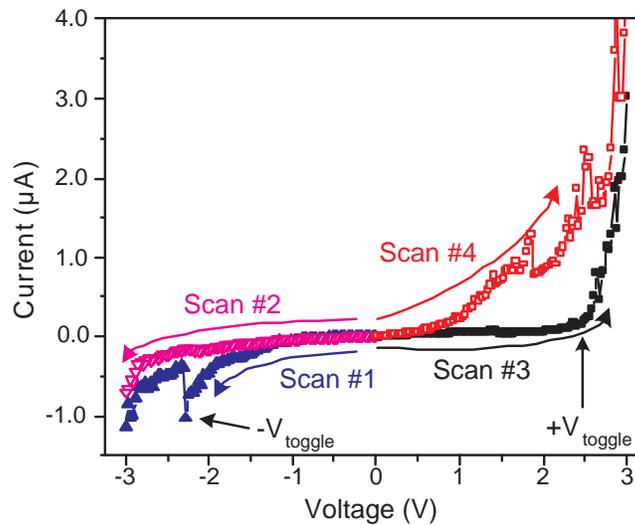


Fig. 3. Room temperature I-V characteristics of nitro molecule monolayer showing switching with memory behavior [Gergel et al. 2005].

2.2 Modeling the Molecular Device for Circuit Simulation

It is clear from inspection of Fig. 3 that this device exhibits a number of non-classical characteristics. One obvious non-classical element is the hysteresis between the high and low conductivity states, however the device in general is very non-linear and is not easily represented by standard SPICE models. Thus, we have chosen to use the universal device model (UDM) [Rose et al. 2004] from the University of Virginia to model the characteristics of our “nitro” device. In general, the UDM models the I-V characteristics of such devices from a set of four possible equations representative of behavior common to nanoscale devices: linear (resistor-like) behavior, thermionic emission (diode equation), resonant tunneling (Gaussian equation) and coulomb blockade (step function). The UDM

is capable of accepting experimental data for devices such as that shown in Fig. 3, and using it to create a Verilog-A model file, consisting of these four types of equations. This model is then utilized by Cadence Spectre during circuit simulations.

2.3 The Crossbar Array Including Applications

As stated previously, the crossbar array is a plane of parallel nanowires crossing another plane of parallel nanowires perpendicularly, with a SAM of molecules sandwiched in between each wire crossing. In general, crossbar-based architectures have several nice features such as programmability, low-cost fabrication and high device densities. Specifically, the regularity of the crossbar structure necessitates only one mask for fabrication. This mask can be used for both sets of nanowires, which greatly reduces fabrication costs.

In this paper, we will study the crossbar array used as molecular memory. As technology advances, memory device density inherently gets larger. The crossbar array gives the ultimate advantage in density, storing one bit at every wire junction in the crossbar. In order to utilize these crossbar arrays as memory structures, we need to create an efficient way to read and write the memory cells. In our $50\text{nm} \times 50\text{nm}$ “nitro” device, the measured currents are typically in the single μA range, giving our devices inherent resistances around $1\text{M}\Omega$. As devices are scaled smaller, these output currents also become smaller, making it hard to determine what exactly is stored in the molecular devices. In fact, it is not uncommon to see device currents on the order of 100pA [Reed 1999; Collier et al. 2000].

In the following sections we discuss methods to optimize the reading and writing process, aiming to assuage limitations posed by inherent device and circuit level characteristics. Since the crossbar array, by itself, is not capable of signal restoration or inversion, some type of CMOS architecture is necessary to perform the read and write functions. Discussed are ways to read and write from CMOS, including methods to augment the crossbar array with CMOS circuitry.

3. CHALLENGES IN DEVELOPING MOLECULAR MEMORY

Using molecular switches for memory seems natural since they are essentially tunable devices that can be set into one of two possible conductivity states, one representing logic ‘1’ and the other logic ‘0’. A device can be written by applying a large magnitude voltage across it where exceeding the positive toggle voltage will force the device into the logic ‘1’ state and a very negative voltage will write a logic ‘0’. Reading can be achieved simply by applying a voltage between the toggle points and measuring the output current (I_{out}). It is for this reason that an important metric of analysis for such a memory circuit is the ratio of the output currents for logic ‘1’ and logic ‘0’, referred to here as the ‘1’/‘0’ current ratio ($F_{1/0} = I_{out1}/I_{out0}$).

3.1 Effects of Large Reverse Bias Currents

To effectively read data from nanoscale memory, the output ‘1’/‘0’ current ratio ($F_{1/0}$) must be as large as possible and must always be greater than one. When this ratio is too small difficulty arises in trying to distinguish a logic ‘1’ from a logic ‘0’. Since it is desirable that $F_{1/0}$ be as large as possible, an important endeavor is the exploration of any device and circuit level factors affecting this ratio.

One device level characteristic directly affecting $F_{1/0}$ is the ratio between the forward and reverse bias currents ($F_{f/r}$) or rectification ratio. The closer $F_{f/r}$ is to one, the closer the device behavior is to that of a resistor. Likewise, device behavior is like that of a diode

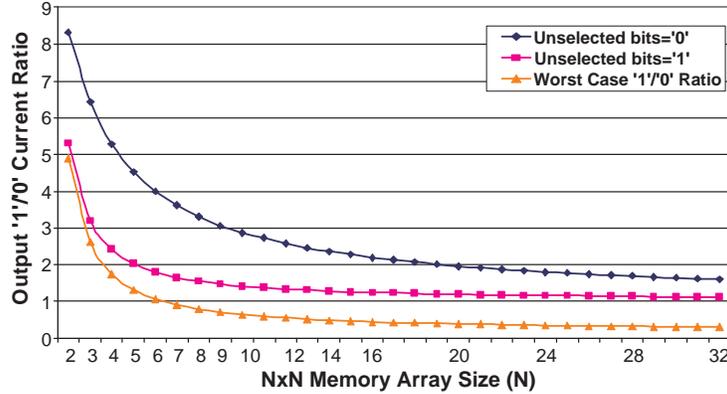


Fig. 4. Maximum array size limited by On/Off ratio of molecular switches.

for $F_{f/r} \gg 1$. Thus, it is this ratio that determines the amount of current that flows through parts of the array that are not selected for reading. This can be understood by considering that as the device is more diode-like ($F_{f/r} \gg 1$), the undesirable nets in Fig. 5 that are parallel to the device being read are essentially cut-off due to the reverse biased diodes.

Looking at it another way, one could model the devices that are reverse biased with a higher resistance than those that are forward biased. By modeling the devices simply as resistors, a resistor network is obtained consisting of the device being read (R_{rd}) in parallel with an equivalent resistance for the unselected devices (R_{unsel}). If the ratio $F_{f/r}$ is close to one, the resistance R_{unsel} is closer to and perhaps smaller than R_{rd} of the selected bit. From this perspective, it can be seen that for a large sized array many devices in the unselected circuit path are in parallel such that R_{unsel} becomes small. In fact, there is a minimum array size at which $R_{rd} \approx R_{unsel}$ leading to a '1'/'0' ratio $F_{1/0} \approx 1$. For larger arrays where $R_{rd} < R_{unsel}$ the current representing logic '0' can be greater than that representing logic '1'.

The point at which the output currents representing logic '1' and logic '0' become indistinguishable can be seen in Fig. 4. In this figure, the output ratio $F_{1/0}$ is plotted against the array size. These results are for the device described in section 2.1 where the ratio between on and off device currents is about 10. The first point to be noticed from this plot is that $F_{1/0}$ is smaller for larger sized arrays showing a limit on array size. Worth noting is that these results assume that all unselected rows and columns are left floating while a bias is applied only to the row and column of the selected device. If the unselected rows and columns are grounded this plot would show a larger maximum array size. It is also worth mentioning that for larger $F_{f/r}$, the ratio $F_{1/0}$ is improved for large arrays. Thus, one way to improve the maximum allowed size of a crossbar memory array is to increase the device property $F_{f/r}$.

3.2 Reading Nanoscale Memory from CMOS

Another important consideration for the design of integrated circuits based on molecular crossbar arrays is that the currents through many molecular devices fabricated to date are much smaller than what is common for conventional bulk Si devices. More specifically, many molecular electronic devices have been fabricated which exhibit measured currents

on the order of nanoamps or even hundreds of picoamps [Reed 1999; Collier et al. 2000]. In an IC composed of both molecular devices and CMOS circuitry, the currents out of the nanoscale circuits may be too small to be accurately sensed using CMOS amplifiers. For the device described in section 2.1, operating currents are actually on the order of microamps, a feature that may make such devices advantageous for circuit development. However, considering that these devices have been fabricated in nanowells with dimensions of about $50\text{nm} \times 50\text{nm}$, it is worth noting that currents through scaled versions of these molecular devices will be much smaller. It is thus important to consider circuit level design techniques for both nanoscale and CMOS circuitry that would allow more tractable methods of reading and writing the memory array. In section 6, a 32×32 molecular memory array is analyzed for various device current magnitudes showing how scaling such devices affect the performance of the memory.

4. DESIGN SOLUTIONS

4.1 Device Level Considerations

As mentioned in section 3.1, array size is limited by the ratio between the forward and reverse bias currents ($F_{f/r}$) through the device. Since a larger $F_{f/r}$ leads to larger maximum array sizes it is worthwhile to explore methods for increasing this ratio at the device level.

Kushmerick et al. [Kushmerick et al. 2004] and Reed et al. [Zhou et al. 1997] have provided evidence suggesting that it is possible to tune the rectification or current-voltage asymmetry either by changing the end group of the molecular device or by changing the actual metal contact [Kushmerick et al. 2004]. In other words, the asymmetry observed in the molecular current-voltage characteristics may be caused by the differences in the metal-molecule coupling at the two contacts. Experiments were performed with a number of different molecular end groups, including the sulfur end group used here, each yielding different asymmetric results [Kushmerick et al. 2004]. Asymmetry has additionally been observed for a symmetric molecule when using Au and Pd as contacts instead of using Au for both contacts [Kushmerick et al. 2004]. This shows that the asymmetry in the contacts can cause asymmetric I-V characteristics regardless of the type of molecule. Theoretically, this Au-Pd contact combination should increase the device rectification ratio for an asymmetric molecular device, such as the nitro device, however more experimentation is needed to verify this.

4.2 Design Options for a CMOS Interface

In order to deal with the potential difficulty in reading a nanoscale memory using CMOS (as described in section 3.2), the proposal described here includes the addition of at least one row of molecular devices that act as load devices to the selected memory bits. More specifically, devices in this extra row are connected to a source voltage on one end and share a column with the selected memory devices on the other such that they are series connected. The signal to be read by CMOS is then a voltage at the node between the device being read and a device in the load row. The voltage across such devices tends to be on an order of magnitude discernible using CMOS circuits making this approach useful to the implementation of hybrid CMOS/nano systems.

An illustration of a nanomemory with a load row is shown in the left of Figure 5. From here it can be seen that to read device D_{11} , a high voltage should be applied at V_{RW} . The voltage then read at node $IO1$ is the voltage across the load device L_1 which is in

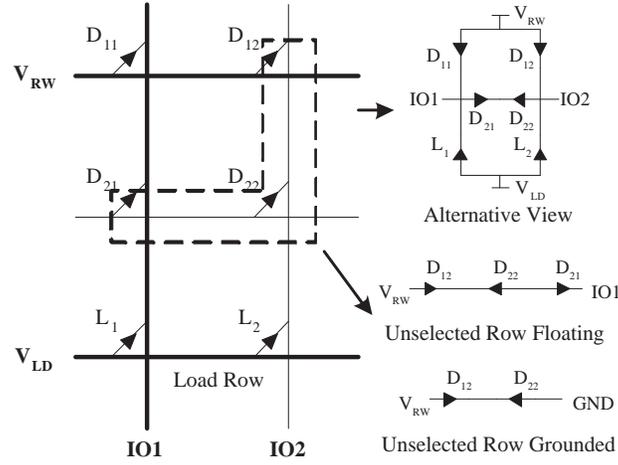


Fig. 5. A 2×2 memory with load row (left) and the undesirable current path in this circuit (right).

Mem. Size	Floating		Grounded	
	worst '0'	worst '1'	worst '0'	worst '1'
2×2	442.4mV	1.188V	59.22mV	1.063V
4×4	915.2mV	1.006V	59.22mV	827mV
8×8	1.109V	787.4mV	59.22mV	596.3mV
16×16	1.119V	572.5mV	59.22mV	394.4mV
32×32	1.243V	390.9mV	59.22mV	239.2mV
64×64	1.265V	256.9mV	59.21mV	134.9mV

Table I. Size limitations for memory where the unselected rows are left floating and the case where they are grounded. Grounding just the unselected rows allows for memory sizes up to at least 64×64 .

series with D_{11} between V_{RW} and V_{LD} (grounded for a read). Since these voltages are on an order of magnitude easily sensed by CMOS, this particular technique allows for easier access to a nanoscale memory.

Ideally, the output voltage only depends on the device being read (e.g., D_{11}) and its corresponding load device (e.g., L_1). This ideal case exists if parameter variations are negligible and all devices along the addressed row are programmed in the same state. If this is the case the voltages at each column are identical and no current flows through the undesirable circuit paths (middle right of Fig. 5). Of course, parameter variations are to be expected and it is unlikely that all bits along a row will be identical. This being the case, current will flow through unselected row devices in such a way that the output signals are degraded. In fact, the size of the array is still limited by the ratio between forward and reverse bias current just like it is when measuring a current at the output as described in section 3.1.

One way to reduce the size limitations of this nanoscale memory is to ground the unselected rows and columns. Given the structure of the memory array when using a load row, a reasonable design might include grounding the unselected rows while the unselected columns remain floating. In the example shown in Fig. 5, the row consisting of devices D_{21} and D_{22} is grounded such that current no longer flows from the path containing $IO2$

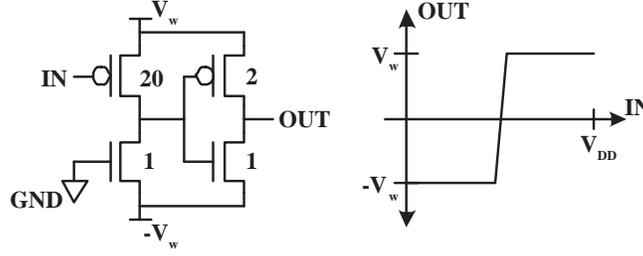


Fig. 7. The CMOS level shifter used at the periphery of the control circuitry to shift V_{DD} and V_{SS} from 2.5V and 0V to 1.25V and -1.25V, respectively.

$$\frac{1}{2} \cdot V_{toggle} \leq V_w < V_{toggle} \quad (1)$$

As a safety net for the circuit, and to ensure the stability of the CMOS control circuitry, extra restrictions should be placed on the write voltage and on the control signal levels. The multiplexors presented in this memory are standard 2-input, pass transistor based muxes, as shown in Fig 6. It is apparent that if V_{dd} is used for the *BitIn* signal (select signal), and a negative write voltage ($-V_w$) is applied to input *B*, the voltage V_{gs} of the NMOS FET in pass transistor 2 will exceed V_{dd} ($V_{gs} = V_{dd} + V_w$), and therefore exceed the breakdown voltage by the amount V_w . Over time this will damage the pass transistor and the device will likely fail.

The following equations present three design criteria that prevent transistor damage and ensure reliable functionality.

$$\begin{aligned} BitIn &= \frac{1}{2} \cdot V_{dd} \\ V_{toggle} &< V_{dd} \\ V_w &= \frac{1}{2} \cdot V_{toggle} \end{aligned}$$

To keep V_{gs} from exceeding V_{dd} while passing a negative voltage, both the input write voltage and the select voltage (V_w) should not exceed $\frac{1}{2} \cdot V_{dd}$. This ensures that $V_g \leq \frac{1}{2} \cdot V_{dd}$ and $V_s \leq \frac{1}{2} \cdot V_{dd}$, and therefore $V_{gs} \leq V_{dd}$. This criterion directly elicits the constraint on the select voltage (*BitIn*) shown above. To ensure the write voltage does not exceed $\frac{1}{2} \cdot V_{dd}$, it is imperative that the toggle voltage is less than V_{dd} . If the toggle voltage is known to be lower than V_{dd} , then applying the constraint above assures $V_s \leq \frac{1}{2} \cdot V_{dd}$, and will thus ensure that $V_{gs} \leq V_{dd}$ for the pass transistor.

This relationship between V_{toggle} and V_{dd} also means that, for the nitro device, V_{dd} must be greater than 2V (V_{toggle} for the nitro device considered). Requiring such a large voltage for V_{dd} affects the choice in CMOS technology used in that the transistors must tolerate these large voltages. For this reason, the simulation results shown here were done using models for the TSMC 250nm process. It is important to note that in order for smaller CMOS technologies to be used, either the FETs should be designed for a higher V_{dd} or molecular devices with a lower V_{toggle} should be used.

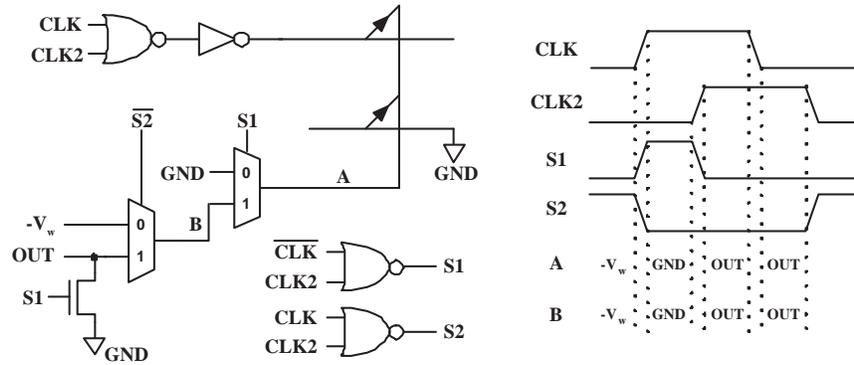


Fig. 8. Illustration of the control circuitry for writing the load devices to the high conductivity state and then reading a selected device (bit) in memory.

4.4 Detailed Memory Operation

During a read, the first step is to force the load device to the high conductivity state by driving V_w on the load row and $-V_w$ on the selected column. Immediately following this, V_w is applied to the selected row in order to read the bit. This could, and usually does lead to a situation where the selected column is holding $-V_w$ just as the row rises to $-V_w$ leading to $2V_w$ across the device which rewrites it. Thus, it is necessary to pull the selected column to ground after writing the load device and before reading the bit. In the case of the design proposed in this work, this is accomplished by using a second clock ($CLK2$) in addition to CLK .

As can be seen in Figure 8, pass-gate logic is used for selecting the appropriate signal to drive onto a selected row or column as well as to connect the selected column to the output during a read. Bidirectional pass-gates are used to both drive signals across the memory lines during a write and to sense the output during a read. The right hand side of Figure 8 shows the timing diagram for this circuitry and how signals evolve on the various nodes in the circuitry used to drive the columns. The diagram shows that immediately after the first step in reading a bit, the column is driven to GND so that the selected device is not overwritten. With the device properly safeguarded, the column is connected to the memory output OUT for the actual read.

The top molecular device in Figure 8 can be considered the memory bit while the bottom device is the load. As can be seen, the row for the memory bit is driven by an inverter such that, during a read, the line is pulled high to V_w (row is selected) or low to GND (row is unselected). It is important to note that such a driver is required for each row in the memory in order to ground all unselected rows. This requirement means that the row decoder is separated from the memory by a CMOS driver such that the decoder cannot be implemented within the nanoscale array itself. However, since the unselected columns are simply left floating, the column decoder can be fabricated using nanowire FETs built into the crossbar array much like has been accomplished at Caltech [Beckman et al. 2005].

4.5 Complete 4×4 Memory and Functional Verification

Fig. 9 shows the complete schematic for the molecular memory architecture proposed in this work. The CMOS column decoder for this memory could be a standard binary or k-

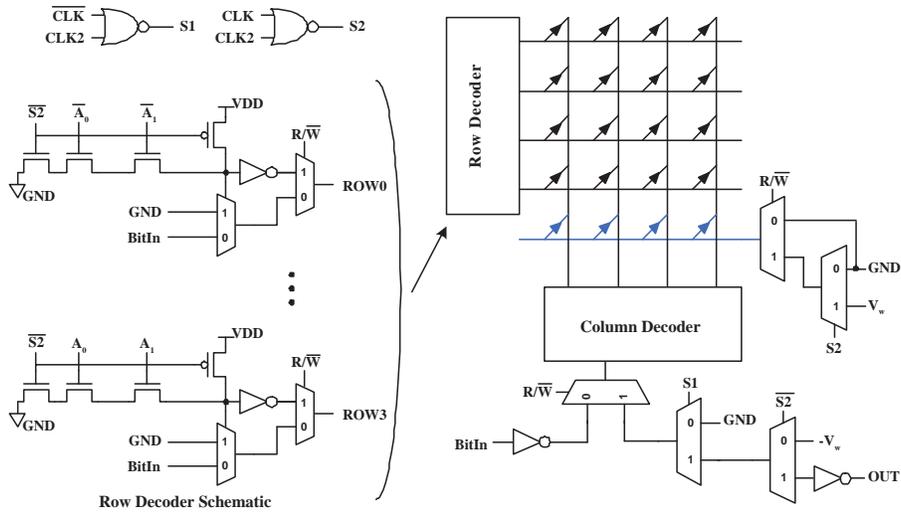


Fig. 9. Illustration of proposed molecular memory architecture complete with required CMOS circuitry. On the right is a high level schematic of the molecular memory complete with decoders and control circuitry to be implemented in CMOS. On the left is a more detailed schematic of the CMOS row decoder including drivers for holding unselected rows to ground during a read operation. The control circuitry for this design makes use of signals $BitIn$, R/W' , and CLK to 1) ensure unselected devices are not overwritten, 2) apply a large enough voltage ($2V_w$) during a write, and 3) ensure the load devices are in a known conductivity state before a read.

hot decoder for selecting a single column. This selected column can then either drive the output or be driven by the appropriate voltage during a write. Similar to the multiplexor based circuitry for the column decoder I/O, the load row is driven with the appropriate voltage depending on whether or not the circuit is reading or writing.

The left side of Fig. 9 shows a more detailed view of the row decoder. This circuit is not very different than what might be used for a SRAM or DRAM with the exception that the write operation requires the $\pm V_w$ voltages. Which of these voltages are to drive the row during a write is determined using the multiplexor circuits shown. Also in the row decoder is the use of a clock signal (CLK) to ensure the row is driven with either V_{DD} (selected) or GND (unselected). The CLK signal appears in the NAND functions of the row decoder implemented using domino logic. The multiplexors for the column decoder and load row also use CLK to force the load devices to the high conductivity state every time CLK goes low during a read. This ensures the conductivity of each load device is known during a read without taking extra time for the operation.

Simulation results for the 4×4 molecular memory array based on the nitro device can be seen in Fig. 10. The simulation first writes to two memory locations: a '0' to '1111' on the top left corner and a '1' to '0000' on the bottom right. These locations were chosen to demonstrate that a write to one bit will not alter the state of other bits in the memory. After the R/W' line goes high for a read operation it can be seen that the correct data has been stored to the two memory locations ('0' to '1111' and '1' to '0000').

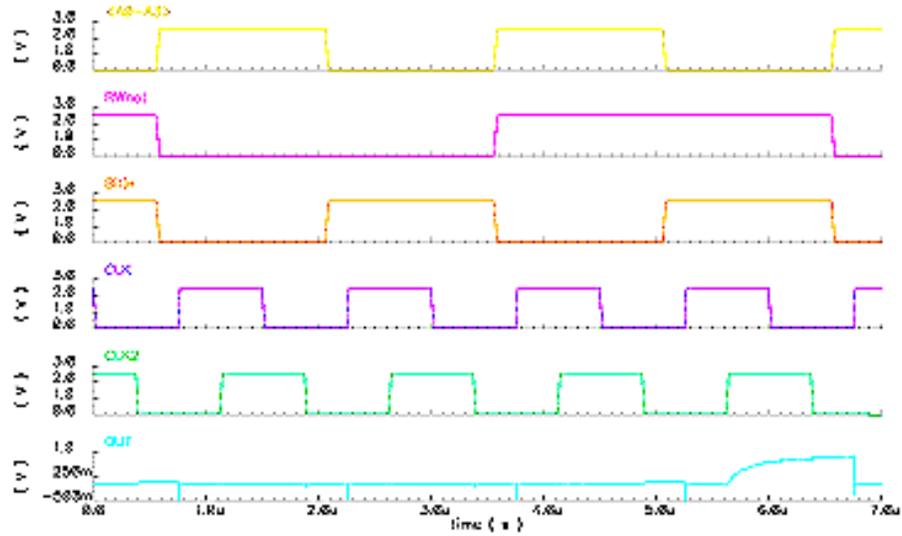


Fig. 10. Simulation results for writing a zero and a one to different locations in a 4×4 nanomemory.

5. DESIGN CONSIDERING VARIATIONS

The previous sections were devoted to designing a memory using ideal hysteretic switches, assuming no variations in device characteristics. Now we will discuss how varying device characteristics can impact the functionality of the circuit, examining the impacts of variations in V_{toggle} and conductance. These simulations are based upon information gleaned from our own experiments, as we want to investigate these variations as realistically as possible.

5.1 An Experimental Perspective on Variations in Molecular Electronics

In order to realize a large-scale functional molecular memory, inter-device variation must be improved. Although circuit modifications may be used to compensate for some variations, as will be described in the following sections, the field is ultimately limited by inconsistencies in the device current magnitudes and toggle voltages. These device variations may be attributed to: irreproducible and impure molecular monolayers due to the prevalent use of a solution-phase molecular assembly method, irregularity in the molecular monolayer resulting from a rough bottom surface, inconsistencies in the top contacts due to the mobility of the metal, and variations in the size of the active device area. However, by improving the molecular device structures and fabrication techniques, device variations may be reduced.

One way to increase device consistency may be to use an improved molecular monolayer assembly method during the fabrication of the devices. Because the functionality of molecular devices depends strongly on the molecular monolayer in the device, the quality and consistency of this monolayer is extremely important to achieving consistent devices. However, the existing method of monolayer assembly, "solution-phase assembly," exposes the monolayers to solvents that can contaminate them. For this reason, a method known as "vapor phase assembly" has been established [Gergel-Hackett et al.]. This solvent-free

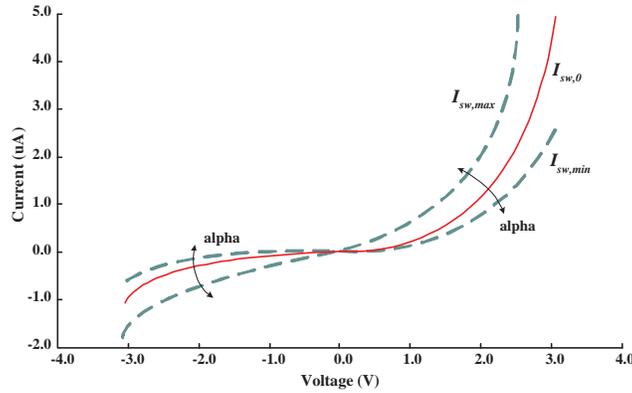


Fig. 11. Conductance variation in a molecular device as defined by the spread factor α .

assembly method utilizes an ultra-high vacuum (UHV) environment and in-situ molecular purification to reduce monolayer contamination.

Additional factors affecting the quality of the monolayer stem from both the top and bottom layers of gold, which provide contacts to the molecular devices. Gold is often a preferred contact choice because it has no native oxide, and molecules which include a thiol linking group (i.e. sulfur) can easily form a strong SAM on its surface. However gold poses a number of problems since it is polycrystalline and has terraces approximately 10-100 nm in diameter (on the magnitude of the molecular device). This means it is likely that a device will deposit along a grain boundary, which causes irregularities in the SAM leading to drastic device variations. Along similar lines, care must be taken while depositing the top gold contact to ensure the energetic metal atoms do not damage the SAM, which could affect the device characteristics.

Previous work observes toggle voltage variations of approximately ± 0.5 V stemming from the issues discussed previously [Gergel et al. 2005]. Also in [Gergel et al. 2005], additional variations are seen in individual device conductance and on/off current ratio, varying from 1:1 to 111:1. The rest of this work will study the impact of these device variations on circuit operation. These previous observed values are used to guide and direct our analyses, aiming to find the maximum allowable variation levels while still maintaining proper circuit operation, and assuring that these devices will provide suitable functionality for the molecular memory.

5.2 Examining the Variation in Device Conduction

In order to choose a value for the read voltage (V_{RD}), it is imperative to ensure that the state of a selected memory bit can be reliably determined at the output. For the CMOS/Molecular memory examined in this work (Fig. 9), all unselected rows and the load row are connected together and tied to ground such that they form a parallel network in series with the selected bit. Since V_{RD} is applied from the selected row to ground via this network, the rest of the array can be neglected in this analysis. Thus, the output voltage of this circuit during a read operation depends on the selected bit and the unselected devices in the same column.

The simplified view described above is important when determining the worst case situ-

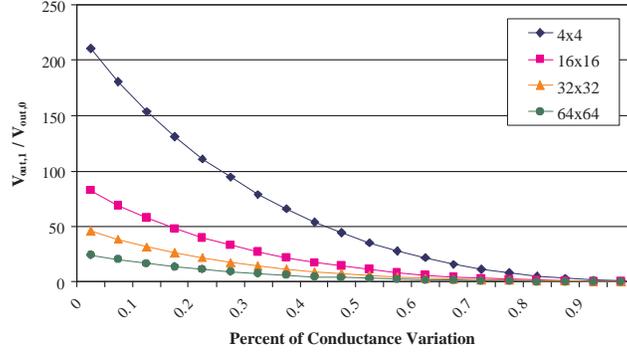


Fig. 12. Worst case output voltage ratio ($V_{out,1}/V_{out,0}$) as a function of the percentage of conductance variations for arrays of size 4×4 , 16×16 , 32×32 , and 64×64 . These simulations were done for the worst case corner for the variation percentage given.

ation in terms of device parameter variations during a read operation. For example, when reading a logic ‘1’ it is clear that the output of the array should be as high as possible. If, however, the conductivity of the devices are allowed to vary it is possible that the impedance of the parallel network consisting of the unselected bits is small enough to lead to a reduced logic ‘1’ output voltage. In fact, the worst case arises when all unselected devices are set in the logic ‘1’ state but have as high of a conductivity value as variations will allow. At the same time the selected bit is also storing a logic ‘1’ but variations, in this worst case, have it’s conductivity at the lowest allowable value. This lower equivalent resistance path to ground, as opposed to V_{RD} , leads to an output voltage that is lower than would be expected without parameter variations. For a logic ‘0’, it can actually be shown that in most cases the output is lower due to variations, and even in the worst case only increases by a negligible amount. It is therefore the worst case logic ‘1’ situation that must be considered to determine the extreme effect of parameter variations on the output.

In order to vary the conductivity of the devices, we setup a few equations for simulation.

$$\begin{aligned}
 I_{sw} &= I_{sw,0} + \alpha \cdot I_{sw,0} \\
 I_{sw,max} &= (1 + \alpha) \cdot I_{sw,0} \\
 I_{sw,min} &= (1 - \alpha) \cdot I_{sw,0}
 \end{aligned}$$

In these equations, I_{sw} represents the device current and α represents percentage of current variation. When observing the first of these three equations, as α increases, the overall device current increases and acts as though the device is more conductive. As α decreases, the current decreases and acts as though the device is less conductive. In our simulations, α may vary anywhere from 0 to 95%. Our aim in varying α is to find the maximum allowable device conductivity variation where the circuit can still function properly, and to simply observe the impact of these conductivity variations on array size. As stated in the paragraph above, when considering the worst case ‘1’, we want the selected device to have as low a conductivity as variations will allow, and we want the unselected bits to have as high a conductivity as variations will allow. To instantiate this, we use the second equation above for the current of the unselected devices, and the third equation for

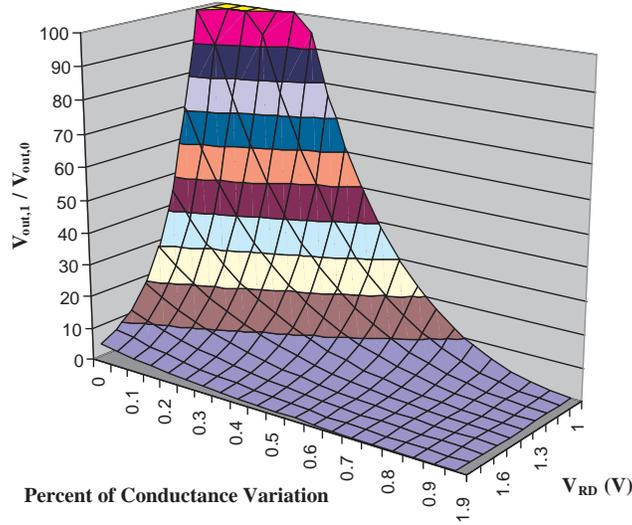


Fig. 13. Worst case output voltage ratio ($V_{out,1}/V_{out,0}$) of a 32×32 array for various read voltages (from 1V to 1.9V) and possible conductance variations.

the selected device. Fig. 13 shows the results when sweeping α from 0 to 95%.

Variations in the conductivity of the devices not only limits the output voltage, but can also have a negative impact on the maximum size of the array. Both of these issues are illustrated in Fig. 12 where the ratios between the worst logic ‘1’ output voltage ($V_{out,1}$) and the logic ‘0’ output ($V_{out,0}$) are plotted as a function of the percentage of variation on device conductivity (in the worst case) for arrays of size 4×4 , 16×16 , 32×32 , and 64×64 . This plot shows that for even the larger arrays, if the conductivity variation is less than ± 0.5 then the output only varies slightly. This gives some indication as to what can be considered acceptable in terms of the conductivity variations for real devices.

Since one purpose of this exercise is to determine a value for V_{RD} that leads to reliable circuits, Fig. 13 shows how the effect of conductivity variations on the output depends on the read voltage itself. This plot is for a 32×32 memory array and shows that for lower values of V_{RD} the output ratio is higher even for a large standard deviation in conductivity variability. The only reason one would not want to simply select V_{RD} as small as possible is that the absolute value of the output voltage must also go down with decreasing V_{RD} until eventually sensing becomes more difficult. It is for this reason that a suitable read voltage for the devices considered in this work might be around 1.3V.

5.3 Effect of Varying V_{toggle}

In addition to variations in the conductance of the devices (or on/off current ratios), the toggle voltages ($\pm V_{toggle}$) will also vary from device to device. In terms of reading data in the array, a somewhat obvious consideration is that the read voltage must be smaller than the smallest possible value for V_{toggle} to ensure bits are never inadvertently overwritten during a read operation. This leads to a design criterion for selecting the read voltage (V_{RD}): $V_{RD} < V_{toggle,smallest}$, where $V_{toggle,smallest}$ is the smallest value possible in the range of toggle voltages. It is worth noting, however, that this criterion should be easily

met if V_{RD} is chosen based on the conductance variation mentioned earlier. Specifically, it was shown that the memory is more tolerable to conductivity variations for smaller read voltages. By choosing a small value for V_{RD} , both criteria will easily met.

The variability of the toggle voltages from device to device has a greater impact on the selection of the write voltage V_w . The criterion for making this choice with *no* parameter variations was described in [Rose et al. 2006] to be:

$$\frac{1}{2} \cdot V_{toggle} \leq V_w < V_{toggle} \quad (2)$$

As can be seen in Fig. 9, during a write operation all unselected rows and the load row are grounded such that nothing more than V_w is applied across the unselected devices at any given time. Since $V_w < V_{toggle}$ according to 2, no devices should switch when unselected. However, consider the case where some unselected device has a varied toggle voltage of the smallest possible value $V_{toggle,smallest}$. Given this possibility, it is wise to modify the above criterion such that $V_w < V_{toggle,smallest}$. Likewise, when writing a particular device, it is possible that the toggle voltage is at the highest possible value $V_{toggle,biggest}$. This being the case, the criterion should again be modified such that $\frac{1}{2} \cdot V_{toggle,biggest} < V_w$. Putting all of this together, criterion 2 now becomes:

$$\frac{1}{2} \cdot V_{toggle,biggest} \leq V_w < V_{toggle,smallest} \quad (3)$$

With the above criterion for V_w given in 3, an important consideration is that it may be possible for $V_{toggle,smallest}$ to be smaller than $\frac{1}{2}V_{toggle,biggest}$ which would prevent a guaranteed safe choice for V_w . This consideration does lead to a simple derivation for the maximum allowable variations on V_{toggle} such that the safety of the write operation is maximized. Consider V_{toggle} can vary by $\pm\beta V_{toggle}$ or from $V_{toggle}(1 - \beta)$ to $V_{toggle}(1 + \beta)$. The maximum value for β is easily found by setting the limits of 3 equal to one another:

$$\begin{aligned} \frac{1}{2} \cdot V_{toggle,biggest} &= V_{toggle,smallest} \\ \frac{1}{2} \cdot V_{toggle}(1 + \beta) &= V_{toggle}(1 - \beta) \\ (1 + \beta) &= 2 \cdot (1 - \beta) \\ \beta &= \frac{1}{3} \end{aligned}$$

Thus, from the above derivation it can be seen that the maximum safe range of variation for V_{toggle} is $\pm 0.33V_{toggle}$.

5.4 Results of Monte Carlo Analysis

A better idea of the effect the discussed parameter variations will have on the memory output has been obtained via Monte Carlo analysis, and the results are shown in Figure 14. These simulations were performed in the Cadence Analog Environment using the Monte Carlo tool to vary certain parameters in a pseudorandom fashion across some spread and then observe the resulting variations on the output voltage. For these particular simulations, the overall conductance was allowed to vary by $\pm 20\%$ and the toggle voltage by $\pm 25\%$. The results after 500 iterations can be seen in Figure 14.

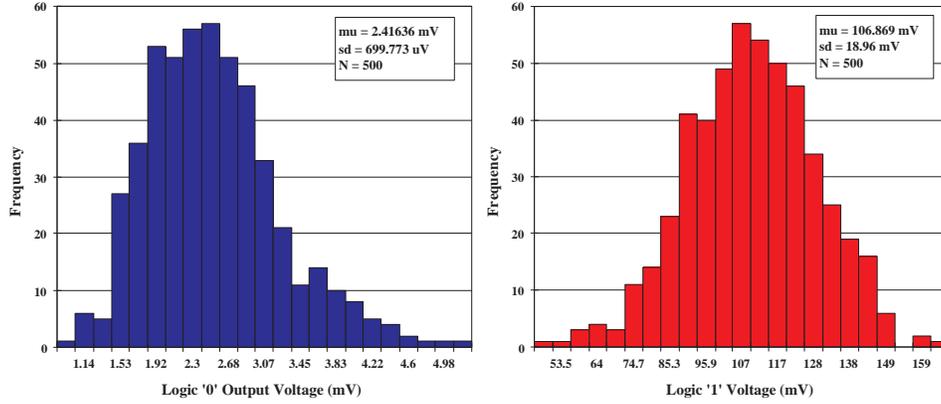


Fig. 14. Monte Carlo analysis results for reading a logic ‘0’ (left) and a logic ‘1’ (right) from a 32×32 memory array. The spreads were assumed to be $\pm 25\%$ for V_{toggle} and $\pm 20\%$ for the overall conductance.

6. PERFORMANCE OF A 32×32 CMOS/MOLECULAR MEMORY

In order to observe the expected performance of a molecular memory built using the nanowell device, a 32×32 or 1 kbit memory array complete with CMOS control circuitry has been simulated. Due to the requirement of somewhat large voltages to read and write most molecular devices, the CMOS circuitry is designed using devices at the 250nm technology node. The use of such relatively large transistors leads to an overall design that is larger than desired but it is important to note that this area is dependent on the CMOS area since the area of the molecular crossbar array is negligible in comparison. For instance, assume the half pitch of the crossbar array is 50nm such that the wire crossings (nanowells) are $50\text{nm} \times 50\text{nm}$ and the wire length between nanowells is also 50nm. Thus, for a 32×32 array of such structures, the area is about $3.2\mu\text{m} \times 3.2\mu\text{m}$ or $10.24\mu\text{m}^2$. Likewise, for 250nm transistors the areas of an NFET and a PFET are roughly $0.35\mu\text{m}^2$ and $0.7\mu\text{m}^2$, respectively. From these sizes for the transistors, the following are determined for the area of each component.

$$\begin{aligned} Area_{INV} &= 1.05\mu\text{m}^2 \\ Area_{NOR} &= 3.50\mu\text{m}^2 \\ Area_{LevelShift} &= 15.5\mu\text{m}^2 \\ Area_{DEC} &= 112\mu\text{m}^2 \end{aligned}$$

From these estimates, the overall area of the CMOS circuitry required to control this molecular memory is about $500\mu\text{m}^2$ ($22\mu\text{m}^2 \times 22\mu\text{m}^2$) using 250nm devices. If 45nm transistors could be used to control the memory even with the large voltages required, the area in CMOS would still be around $90\mu\text{m}^2$.

The simulation results for writing and reading two locations in the memory can be seen in Figure 15. This figure is very similar to what is shown in Figure 10 except that the clock is about ten times slower for the 1 kbit memory than for the 16 bit memory. This slow down can actually be understood since the capacitance and thus the delay of the memory

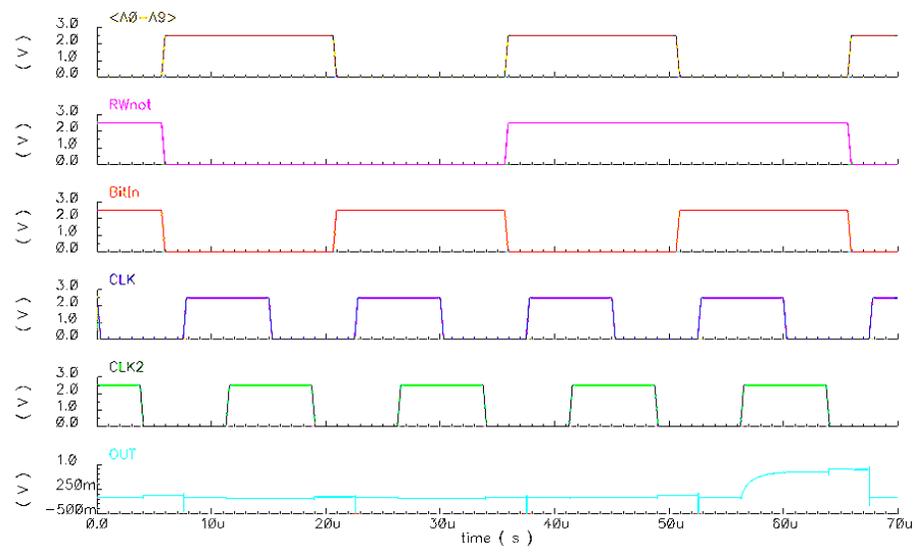


Fig. 15. Simulation results for writing and reading a 32 × 32 (1 kbit) molecular memory.

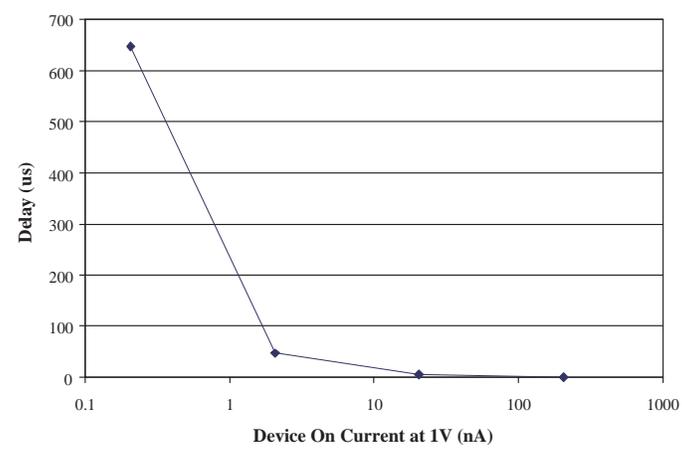


Fig. 16. Delay through a 32 × 32 memory array as the current magnitude of the nitro device scales.

is increased with the size of the memory. Just as the delay increases with increasing array size, scaling the size of the nanowells leads to lower currents through the individual molecular devices and also increases delay. The plot in Figure 16 how the delay of the 32 × 32 memory depends on the current magnitude through each molecular device. The x-axis lists a parameter *SCALE* which is used to scale the overall conductance of the molecular device. The current through a nitro device with 1V applied across it is about 205.7pA for *SCALE* = 1, about 20.57pA for *SCALE* = 0.1, and so on. As can be seen in the plot, the delay increases by a little more than a factor of 10 as *SCALE* decreases by the same factor. Such large delays can be discouraging unless other factors such as power are also

taken into consideration.

From the simulations of the 32×32 memory array, the average power for reading the memory remained around 1.52mW when using the level shifter shown in Fig. 7 to adjust the rails of all input signals. Since the level shifters are expected to consume a lot of static power (there always exists a path from V_{DD} to ground), it is useful to determine the power when they are not present. Without the level shifters and with all inputs swinging between $-V_w$ and $+V_w$, the average power consumption was found to be about $110\mu\text{W}$ when the device on current at 1V was 205.7nA. Due to the small currents through the devices, one might expect this value to be smaller. However, these values are reasonable considering that the voltages driven across the array for both a read and a write are on the order of 1-2V as opposed to a few hundred millivolts for some other technologies. As was discussed in section 4, the voltage for a write must be larger than V_{toggle} in order to write and for the nitro device (as well as many other molecular electronic devices) V_{toggle} is about 2V. Furthermore, the read voltage is usually half of what is applied for a write since this means fewer voltage supplies require distribution. The results also show that the circuitry consuming most of the power is in the CMOS layer and not at the nanoscale where power is negligible in comparison. In fact, after analyzing the crossbar array *without* the CMOS circuitry, the average power consumption of the memory was found to be about $3\mu\text{W}$. Based on these results it can be concluded that molecular electronics can be used for extremely low power memories but the design of any CMOS interface circuitry must take care to operate at low power as well.

7. CONCLUSION

This work has identified specific merits and potential issues when using molecular electronic devices in a hybrid CMOS/Nano memory circuit. Design solutions are described which address discussed limitations from both the device and circuit levels of abstraction. Specifically, from the circuits perspective, it has been shown that molecular devices can be used to load addressed memory such that the CMOS interface deals only with voltages and not currents. Such a design choice leads to CMOS circuitry that does not have to be as sensitive as would be required to sense the small currents (100pA) typical of molecular electronics.

This work shows that, from the perspective of circuit operation, integrating CMOS and nanoelectronic devices on the same die is feasible. Important to note, however, is that as the field of molecular electronics matures, device and circuit level properties and potential limitations (e.g., yields and parameter variations) will become more fully characterized. Future study will consist of including such characterizations in the simulation of memory circuits for accurately evaluating the effects of parasitics, noise, and parameter variations.

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