

Silicon-Based Semiconductor Heterostructures: Column IV Bandgap Engineering

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Invited Paper

Semiconductor heterostructures greatly enhance the range of possible device configurations and open the door to new physical phenomena such as tunneling, tunable optical absorption, real space carrier transfer, two-dimensional carrier gases, and quantum size effects. Because silicon had no natural semiconductor partner, exploitation of these effects had been confined to compound semiconductors. By use of strained layer epitaxy, we have now learned how to grow high quality $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ heterostructures and have applied these materials to a wide range of heterostructure devices. This paper reviews the mechanisms of strained layer growth, the bandstructure of the resulting material, and its use in test devices, including superlattice avalanche photodiodes for fiber optic communication, intra-subband optical detectors and arrays operating in the 10–15- μm wavelength range, mobility enhanced modulation-doped transistors, heterojunction bipolar transistors with cutoff frequencies of 75 GHz, and negative resistance devices based on resonant tunneling and real space carrier transfer.

I. INTRODUCTION

In the earliest semiconductor devices, carrier flow was defined by the spatially controlled introduction of dopant impurities. These “homojunction” devices include the bipolar and MOS transistors that provide the foundation for modern semiconductor electronics. In the last two decades, many researchers have turned to “heterojunction” devices that supplement homojunction control by the use of multiple semiconductor materials within a single device. Heterojunctions can be used to drive both carriers into the same volume, or to separate carriers from the parent dopant atoms, or to form local accumulation or depletion regions, independent of doping. This behavior contrasts sharply with homojunctions where, at rest, electrons and holes accumulate only in those regions defined by their parent donor and acceptor impurities.

The heterojunction offers an immensely larger array of device configurations and has become the basis for the so-called field of bandgap engineering [1], [2]. Nevertheless, it is estimated that heterojunction devices account for no more than a few percent of current semiconductor

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production. The discrepancy stems from the fact that the dominant semiconductor, silicon, is not naturally compatible with any other semiconductor. Heterojunction devices have thus been based on the use of column III–V and II–VI compound semiconductor materials. Compared to silicon, these materials are at least ten times more expensive, they have inferior mechanical and thermal properties leading to smaller, less flat wafers of lower crystalline perfection, and they lack a native oxide that has anywhere near the electrical or chemical quality of SiO_2 [3]. These compound semiconductor heterostructures have thus achieved robust commercial success only where they produce results physically impossible in silicon, such as the emission of light. Although this state of affairs may satisfy certain silicon chauvinists, it is frustrating that proven heterojunction concepts cannot find wider utility. The obvious solution is to bend nature’s rules to find another semiconductor that can be made compatible with silicon. In a very literal sense, that is the topic of this review.

II. LATTICE MATCHED SEMICONDUCTORS

Heterostructures are based on differences in the electronic bandstructure of the component semiconductors. As a free carrier approaches a heterostructure boundary, it should be influenced only by these potential gradients. It should not be trapped or artificially scattered, nor should the heterostructure boundary be the source of leakage currents or other spurious effects that will degrade device performance. In general, this means that the atomic bonding of the component semiconductors must be maintained without interruption across the heterojunction. This condition, in turn, implies that both the atomic arrangement and atomic spacing of the two semiconductors must be essentially identical. If this were not the case, misbonded or incompletely bonded interfacial atoms would contribute interfacial electronic states in the same way unpassivated silicon atoms contribute surface states at a Si/SiO_2 interface. A discussion of possible silicon-based heterostructures must, therefore, start with a large dose of crystallography and crystal growth.

All of the common semiconductors are based on four-fold tetragonally oriented bonds, generally arranged in a diamond-like configuration. The problem is, therefore, reduced to that of identifying another semiconductor with silicon's atomic spacing but with a bandstructure sufficiently different that carriers will be strongly influenced by the heterojunction. The key parameters, lattice constant, a_0 , and minimum bandgap are plotted in Fig. 1. An ideal semiconductor heterojunction should employ semiconductors lying along a vertical line in this figure. Historically, the obvious heterostructure choice was the pairing of GaAs and AlAs. These materials not only share one constituent atom but have lattice spacings matched to within 0.1%. Further, they can be combined in alloys of $\text{Al}_x\text{Ga}_{1-x}\text{As}$, where the Al fraction, x , may be varied to give a range of bandgaps from 1.5 to over 2 eV.

It would appear that a silicon-based analog of GaAs/AlAs could be built on a pairing with either GaP, AlP, or ZnS. Several problems have persisted, however. To grow a crystalline heterostructure, atoms must have sufficient mobility that they can move to properly coordinated crystalline sites. This implies a certain minimum level of heating, which in turn introduces the possibility of solid state diffusion. GaP, AlP, and ZnS are composed of precisely those atoms that produce electrical doping in Si (and vice versa). Diffusion of the constituents across the heterojunction boundary leads to unintentional doping and, frequently, to p-n junction formation. If thermal cycles are controlled well enough, diffusion lengths can be calculated, and in principle this unavoidable cross-doping could be incorporated into the heterostructure device design.

Unfortunately, interdiffusion is not the only problem. As silicon is grown, most III-V dopant atoms have a tendency to segregate on its surface [4], [5]. This occurs because a condensing Si atom has a finite probability of exchanging positions with a surface dopant atom. The process is driven by the fact that silicon has a very strongly bound lattice and the differences in the dopant atom size and electronic structure substantially perturb this structure. If the normal processes of lattice vibration and atomic rearrangement present the surface with the possibility of expelling a dopant in favor of a silicon atom, this option will often be exercised. The net result is that when silicon is grown on a material such as GaP, surface reservoirs of Ga and P can develop and persist to large silicon layer thicknesses. The gradual depletion of these reservoirs produces low level cross-doping not only on the scale of diffusion lengths but to distances of micrometers or more [6]-[8].

If these problems were not enough, silicon-based heterostructures can display another extremely annoying tendency: they may not grow as layers. Si and GaP share the same atomic structure and spacing, but as column IV and III-V semiconductors, their bonding is still significantly different in character. Si bonding is covalent; GaP bonding is somewhat polar. The interfacial bonds between the GaP and Si layers may, therefore, be highly energetic. If their energy is higher than that of bonds at a GaP free surface, rather than lay down as smooth layers, GaP may grow as

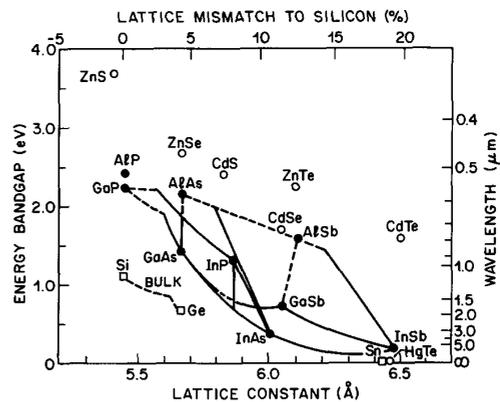


Fig. 1. Plot of semiconductor lattice constants, a_0 , versus minimum bandgap, E_g , for the common semiconductors. Lines indicate bandgap for alloy of semiconductors at end points. Solid line denotes a resulting direct minimum bandgap, dashed line an indirect bandgap. Also shown are photon energies equivalent to the minimum bandgap and percentage lattice mismatch to silicon's 5.43 Å lattice constant.

isolated, three-dimensional islands [9], [10]. This process is precisely analogous to the beading of water on a clean smooth surface. If one persists long enough, the island sizes will eventually grow to the point that they will coalesce and form continuous layers. Typically, however, this condensation occurs at thicknesses ranging from 10's to 100's of nanometers. Not only does morphology place a limit on minimum layer thickness, but the islanded semiconductor is continuously exposed to volatile species from the partially uncovered substrate semiconductor and may thus be unintentionally doped at high levels throughout its volume.

Taken together, the above effects mean that although silicon can be grown with lattice matched, chemically dissimilar materials, controlled structures are generally achieved only with individual layer thickness on the order of 1 μm or more. This effectively eliminates the vast majority of potential heterojunction devices and leads one to consider the possibility of a lattice mismatched but chemically similar semiconductor pairing.

III. MISFIT ACCOMMODATED $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ HETEROSTRUCTURES

Based on their structure and the maturity of their technologies, the natural column IV pairing is of Si with Ge. Germanium has an atomic spacing 4.2% larger than that of Si. The epitaxial growth of Ge on Si can proceed to either of the configurations illustrated at the right of Fig. 2. As the first few atomic layers of Ge are deposited, it is energetically desirable that they maintain full bonding with the silicon by compressing together, as illustrated by the "Strain" configuration at the bottom right. Because the Si substrate lattice is both much thicker and stiffer, it is essentially undistorted. As the thickness of the Ge increases, so does the integrated strain energy and at some point this

configuration will reach a total energy larger than that of an alternate arrangement labeled “Misfit” at the top right of the figure.

In the misfit configuration, the bulk of both layers remains strain free, and the lattice mismatch is accommodated by distortions near the interface and by periodic arrays of incompletely bonded atom rows known as misfit dislocations. Because atoms on these misfit dislocations have three rather than four bonds, the remaining dangling bond can become a trap or leakage site. Such dislocations are clearly to be avoided within the active volume of a device. In principle, the array of misfit dislocations can be confined entirely at the epitaxial interface, as suggested by the figure. This would mean that essentially ideal layers of Si and Ge could be spliced together, despite the presence of a less than perfect interface. An analogous configuration is frequently proposed for GaAs on Si (and has been the source of much misplaced enthusiasm). Unfortunately, this view ignores the realities of crystal growth. In Fig. 2, the misfit configuration can be created by taking the strain configuration, deleting the plane of epitaxial atoms indicated by the dark bonds, re-establishing bonding across the interface and allowing the strain to relax. During crystal growth this deletion can occur by either the accumulation of lattice vacancies or by an equivalent rearrangement of atomic bonds. The important point is that relaxation occurs by deletion of a *plane* and that, within the crystal, the plane must be bounded by at least one row of misbonded atoms. In the heterojunction, the boundary is the misfit dislocation identified in the top right cross section of Fig. 2. However, as depicted in Fig. 3, the edges of such a plane define two additional dislocation segments called threading dislocations because they run through the thickness of the epitaxial layer (and, therefore, through the heart of any heterostructure device).

Many strategies have been attempted to minimize the density of threading dislocations in such misfit accommodated epitaxial layers. The first possibility is extending the dislocation plane either to the edge of the wafer or at least to the boundary of a device die where threading dislocations would be irrelevant (Fig. 3 at left). By annealing $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ samples within a transmission electron microscope, extensive measurements have now been made of the rate at which such planes nucleate and grow [11], [12]. At typical epitaxial growth temperatures of 550°C , dislocation planes extend laterally at a velocity of $0.01\text{--}1.0\ \mu\text{m/s}$ and would thus require about 5 h to grow across a 1-cm die. This process accelerates sharply at higher temperatures, but so does the nucleation of new dislocation planes and the balance is still driven toward having numerous planes, each with a pair of threading dislocations (Fig. 3, center). A second approach acknowledges the nucleation of numerous planes but proposes that structures, such as strained layer superlattices, might cause such planes to grow together and consolidate (Fig. 3, at right) [13]. With each consolidation event, a pair of threading dislocations would be eliminated. This idea has proven to have validity in reducing very high threading dislocation densities to more moderate levels (e.g., driving a $10^9/\text{cm}^2$ density to $10^6/\text{cm}^2$). However,

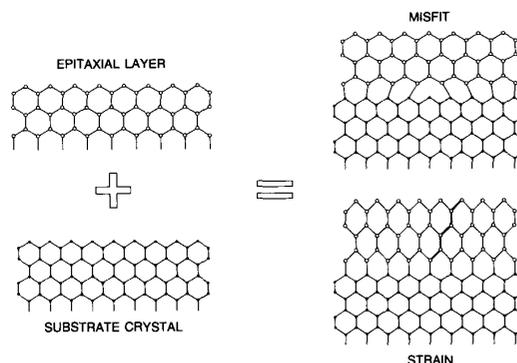


Fig. 2. Schematic representation of alternate growth modes for two lattice mismatched, tetragonally bonded, semiconductors. At left, both materials in their bulk, undistorted form. Bottom right: strained layer growth mode typical of thin layers where the epitaxial layer compresses in the growth plane to match the substrate lattice atomic spacing. Top right: misfit dislocation growth mode typical of thick mismatched layers where epitaxial layer has returned to its bulk, undistorted, form by introduction of misfit dislocations (misbonded atom rows) at the heterojunction interface. Note that the strained configuration is converted to the misfit configuration by the deletion of a plane of epitaxial atoms equivalent to those connected by the dark bonds.

below these levels, not only are further planes unlikely to combine, but repulsive forces between dislocations provide a barrier to such consolidation [14]. Another possibility is high temperature growth of very thick (e.g., $5\ \mu\text{m}$), compositionally graded, misfit epitaxial layers [15] or the collection of threading dislocations in well-defined regions by overgrowth on oxide patterns [16]. Although research along these lines will continue, to date no experiment has produced misfit accommodated growth with threading dislocation densities near those expected in state of the art silicon circuits and with the layer thicknesses needed in a true heterostructure device.

IV. STRAINED LAYER $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ HETEROSTRUCTURES

The above discussion shows clearly that it would be far more desirable to retain the “Strain” configuration depicted at the bottom right of Fig. 2. In the late 1940’s, a formalism [17]–[19] was developed to calculate the thickness at which a strained epitaxial layer would acquire an energy greater than that of a misfit accommodated layer and thus become unstable. As applied to Ge on Si (or alloys of $\text{Ge}_x\text{Si}_{1-x}$ on Si), this model predicted that only very thin layers, 20–30 nm or less, could be grown before the onset of misfit dislocations. Not only did early experiments [20]–[22] appear to confirm these calculations but it was reported that $\text{Ge}_x\text{Si}_{1-x}$ on Si could not be grown with more than 15% Ge without the alloy layers balling up into discontinuous nuclei as is observed with III–V on Si growth. While such islands would not be vulnerable to vapor phase doping as in the III–V on Si case, one would nevertheless lose the capability of thin layer growth for these compositions. Within the 0%–15% Ge range, viable heterostructure devices are still conceivable if a

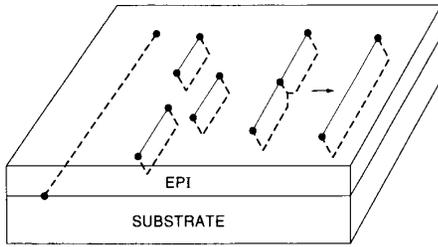


Fig. 3. Schematic three-dimensional representation of the formation of misfit dislocations by deletion of atomic planes. Dislocation lines denoted by dashed lines. Left: Ideal situation where plane extends all of the way to the semiconductor boundary. Center: Actual configuration where numerous short dislocation planes are nucleated, each with a misfit dislocation segment in the hetero-junction plane and two threading dislocation tails propagating up through the epitaxial layer. Right: Possibility of two short planes combining to form a larger plane, thereby eliminating two threading dislocation segments. Note, actual dislocation planes could be tilted $\pm 60^\circ$ and would run in two perpendicular arrays.

fundamental criterion is met: that there is a sufficiently large difference in bandgap between the layers that carriers will be confined. At the time of these experiments, it was believed that the bandgap of $\text{Ge}_x\text{Si}_{1-x}$ epitaxial layers would follow the upper solid line in Fig. 4 [23]. It is evident that if one were limited to normal 15% alloys, a maximum bandgap difference of only about 60 meV would exist between the alloy and Si. As this would be divided between conduction and valence bandedges, only very weak carrier confinement might be possible at room temperature (i.e., $60 \text{ meV}/2 \sim kT$). Early $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ experiments gave no indication that these bulk alloy bandgap data were not applicable, and work on this system was largely abandoned.

In the early 1980's, we reexamined $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ strained layer epitaxy using improved techniques of molecular beam epitaxy (MBE) [24], [25]. In contrast to earlier work, we found that, at low growth temperatures (600°C), it was possible to grow smooth continuous layers of all $\text{Ge}_x\text{Si}_{1-x}$ compositions on Si (up to and including pure Ge). Further, strained layer growth could be maintained to thicknesses much greater than earlier predictions or measurements. Indeed, for dilute alloys, thicknesses of $100 \text{ nm} - 1 \mu\text{m}$ were achieved. This capability is illustrated dramatically by the cross-sectional transmission electron micrograph [26] of Fig. 5 showing a superlattice of superlattices. In this figure, the dark bands are Ge layers and light bands are composed of smaller light/dark bands corresponding to alternating layers of Si and Ge only four and six atomic planes thick. All layers are smooth and continuous, as confirmed not only by such images but by the superimposed electron diffraction pattern and X-ray scattering measurements. The quality and perfection of such structures are comparable to the best achievable in conventional III-V or II-VI heteroepitaxial semiconductor systems.

Subsequent experiments [27] showed that the enhancement in maximum strained layer thickness does not, in fact, contradict equilibrium theory but stems from the fact that, at low temperatures, thick strained films are kinetically limited

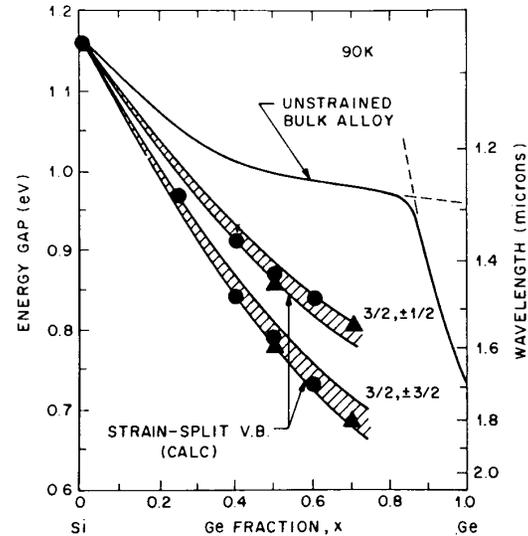


Fig. 4. Bandgap data for $\text{Ge}_x\text{Si}_{1-x}$ measured at 90 K. Top line is for normal unstrained alloys. Bottom bands calculated for strained alloy layer grown on undistorted silicon. Difference between bands stems from strain splitting of the valence band energies. Data points are from optical absorption measurements of strained layers. Data measured at 90 K for signal to noise improvement. Room temperature values can be calculated by using (1).

from achieving a lower energy misfit accommodated configuration. Although these thick layers are thus metastable, they can be processed at temperatures of $800^\circ\text{C} - 1000^\circ\text{C}$ without strong strain relaxation. A modern mapping of $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ growth modes is thus represented by Fig. 6. This map is divided into three regions: at the lower left are those thicknesses and compositions for which strained, dislocation free is the equilibrium growth mode; in the middle is a region where, at low growth and processing temperatures, strained layer growth can be achieved, but as a metastable form; and finally, at the upper right is a region where misfit dislocation formation cannot be avoided. For fairly obvious reasons, the upper bounds of the equilibrium and metastable regions are referred to as equilibrium and metastable critical layer thicknesses (L_c). The metastable critical thickness is temperature dependent and is here drawn for layers grown at 550°C . Although it may seem counterintuitive, it must be stressed that, within the equilibrium strained region, dislocations do not form and will not form, even on subsequent thermal processing because their formation represents an increase in energy over the strained configuration. The above data were obtained with MBE films, but it has since been demonstrated that comparable results can be achieved if chemical vapor deposition (CVD) growth is conducted in the same temperature range [28], [29].

Figure 6 provides guidelines for the design of a single set of $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ layers, but does not indicate what limits would apply to a multilayer structure, as might be called for in a heterostructure device. A generalization of these limits is based on experimental observations of the way



Fig. 5. Transmission electron microscope cross section of $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ strained layer superlattice of superlattices. Dark, wide, bands are 250 Å thick Ge layers. Lighter bands consist of alternating layers of four Si atomic planes and six Ge planes. These atomic layer dimensions are confirmed by faint superlattice spots appearing in inset electron diffraction pattern.

in which a very thick multilayer structure relaxes to form misfit dislocations [30]. Figure 7 shows the transmission electron micrograph of a 100-period $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ strained layer superlattice. As such a structure is grown or processed, one might expect misfit dislocations to form at each strained layer interface, thereby relaxing the metastable strain in every layer. Analysis of this image shows that this does not occur and that, instead, initial relaxation occurs primarily at the bottom-most superlattice to substrate interface. The entire superlattice acts as a single layer, relaxing as a unit when its integrated strain energy exceeds the alternate misfit accommodated configuration. This results in an alternating, or “symmetric,” strain configuration with the partially relaxed $\text{Ge}_x\text{Si}_{1-x}$ layers under compression and the interleaved Si layers under tension. Based on this analogy to a single layer, a stable strained multilayer $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ structure can thus be grown if two rules are followed: 1) every $\text{Ge}_x\text{Si}_{1-x}$ layer within the structure must be stable (or metastable) according to Fig. 6 and 2) a hypothetical layer of the multilayer’s total thickness and volume averaged Ge fraction must also be stable. (Note that if the individual $\text{Ge}_x\text{Si}_{1-x}$ layers are metastable, they may eventually relax upon extended thermal processing, with the generation of misfit dislocations at each interface.)

V. $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ BANDSTRUCTURE AND BAND ALIGNMENT

The above findings solve the first part of the silicon-based

heterostructure problem: the identification of a semiconductor pairing that is viable on crystallographic and doping grounds. The second requirement is that the semiconductors have bandstructure differences large enough that free carriers will be strongly affected. The early bandgap measurements of Fig. 4 left this point in doubt. Fortunately, synthesis of these much thicker $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ strained layers permitted the first measurements of strained layer bandgap and band alignment. Because these layers contain distortions comparable to that which would be achieved by applied pressures of 100 000 atm, it was predicted [31] that they might have a bandgap radically narrower than that of the bulk, undistorted alloys. Optical absorption measurements [32] on $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ photodiodes confirmed these calculations as indicated by the data points of Fig. 4. The lower (more device relevant) band of strained data can be approximated by the relationship:

$$E_g(x, T) = E_o(T) - 0.96x + 0.43x^2 - 0.17x^3 \quad (\text{eV}) \quad (1)$$

where E_g is the difference between the lowest lying conduction bandedge and highest valence bandedge for an alloy layer, $\text{Ge}_x\text{Si}_{1-x}$, strained to grow on an unstrained Si layer (or substrate), and $E_o(T)$ is the bandgap of bulk Si (1.17 eV at 90 K or 1.12 eV at room temperature). This equation shows that a $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ heterojunction with as little as 10%–20% Ge will have a net bandgap difference approaching 200 meV (or 8 times kT at room temperature)

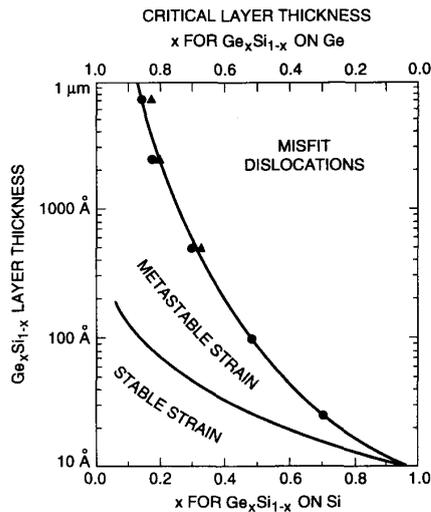


Fig. 6. Limits of strained layer (defect-free) growth for $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ on (100) Si. Top Right: those thicknesses for which layer thickness and/or Ge fraction is too large to be accommodated purely by strain and misfit dislocations form. Center: configurations in which strained layer growth can be produced at low temperatures but for which strain is metastable and relaxation may ultimately occur upon extended thermal processing. Bottom Left: configurations for which strained layer growth is the lowest energy state and for which dislocations will not form. Upper limit of this equilibrium domain is based on calculations which differ slightly based on underlying assumptions.

and will thus produce strong confinement of at least one type of carrier.

To completely determine the degree of carrier confinement, one must ascertain how the net bandgap difference will be divided between the valence and conduction band-edges. This partitioning had been calculated by various methods with widely differing results [33], [34]. It was resolved experimentally using the modulation doping effect in which one layer of a $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ pair is doped either n- or p-type and the conductivity of the sample measured as a function of temperature. At very low temperatures, the free carriers in a uniform layer will eventually fall back into the energy states defined by the parent donor or acceptor impurities leading to carrier “freeze-out.” In a modulation-doped semiconductor, freeze-out will not occur if the free carrier in a doped layer finds a lower energy state across a heterojunction. The earliest measurements of modulation-doped $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ structures [35], [36] showed strong low temperature conductivity if a p-type Si layer was grown adjacent to an undoped $\text{Ge}_x\text{Si}_{1-x}$ layer, weak conductivity for n-type Si on $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$, and freeze-out in all other configurations. These results indicated that the difference in bandgap was divided approximately 80%–20% between the valence band and conduction band discontinuities, as indicated at the top of Fig. 8. In this configuration, those carriers leaving the doped layers are still attracted to the heterojunction by the electrical charge of the donors or acceptors, tending to form n- or p-type quasi-two-

dimensional layers, as shown at the center of the figure. The existence of such two-dimensional layers was confirmed by magnetoresistance measurements displaying Shubnikov de Haas oscillations at those magnetic field strengths where the cyclotron resonance energy equaled the energy separation between the Fermi level and an energy level of the quantum confined 2-D charge layers.

A year later, investigators reported that, in structures similar to those of Fig. 7, carriers transferred from n-type $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ to adjacent undoped Si [37], [38]. This would indicate that the conduction band of $\text{Ge}_x\text{Si}_{1-x}$ is above that of Si, contradicting the upper portion of Fig. 8. The difference was shown [39] to stem from the fact that a thick structure may relax to form a symmetric strain configuration where interleaved Si layers are under tension. The shift in the strain configuration changes the bonding energies of the layers, altering the relative band alignments, as indicated at the bottom of Fig. 8. The band discontinuities for both configurations can be deduced from Fig. 9, or from the relationship:

$$\Delta E_v(x, y) = [0.84 - 0.53y]x \quad (2)$$

where ΔE_v is the difference in valence band energies (in electron-volts) between adjacent $\text{Ge}_x\text{Si}_{1-x}$ and Si layers grown with an in-plane lattice constant equaling that of an unstrained $\text{Ge}_y\text{Si}_{1-y}$ buffer layer (or substrate). The most general case of $\text{Ge}_x\text{Si}_{1-x}$ on $\text{Ge}_z\text{Si}_{1-z}$, lattice matching a $\text{Ge}_y\text{Si}_{1-y}$ substrate, can be calculated by subtracting the values for $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ on $\text{Ge}_y\text{Si}_{1-y}$ and $\text{Ge}_z\text{Si}_{1-z}/\text{Si}$ on $\text{Ge}_y\text{Si}_{1-y}$. Although the relaxed, symmetrically strained configuration substantially augments the possible heterostructure designs, such relaxation occurs only by the formation of misfit dislocation planes with all of the attendant problems of threading dislocations described in Section III.

VI. DEVICE APPLICATION OF $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ HETEROSTRUCTURES

$\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ device work is still in its infancy. Nevertheless, of the nonlight emitting heterostructure devices in the compound semiconductor literature, most have now been demonstrated in this silicon-based system. These include quantum well photodetectors, modulation-doped transistors, and heterojunction bipolar transistors, along with limited reports of more exotic tunneling and intrasubband devices. Aside from the obvious validation of this silicon-based heterostructure system, these test devices provide important information on the suitability of these materials to standard silicon device processing.

A. Optical Detectors

$\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ has been used to produce research photodetectors in two principle wavelength ranges. In p-i-n devices, Ge-containing layers have extended the normal Si absorption edge of $1 \mu\text{m}$ out to $1.3\text{--}1.5 \mu\text{m}$ where silica communications fibers have the lowest losses. Other studies have used heterostructures in various configurations

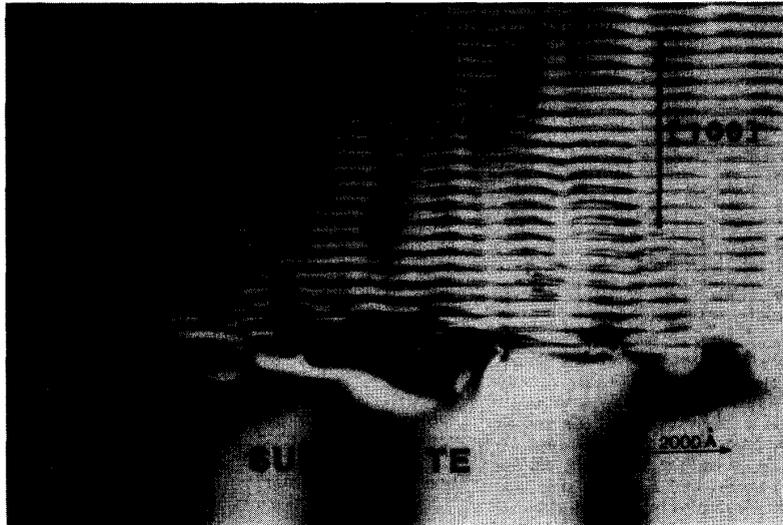


Fig. 7. Transmission electron microscope cross section showing substrate and part of a one hundred period $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ strained layer superlattice. This superlattice is so thick that it has relaxed by the formation of misfit dislocations at the boundary between the substrate and the superlattice, as indicated by the irregular dark/light bands. After this relaxation, the in-plane compression of the $\text{Ge}_x\text{Si}_{1-x}$ layers is partly relieved by stretching of the interleaved Si layers. The resultant alternating compression/tension strain field fundamentally alters the alignment of the $\text{Ge}_x\text{Si}_{1-x}$ and Si bandedges.

to provide silicon-based far infrared detection for survey, surveillance and medical applications.

For fiberoptic applications, the data of Fig. 4 suggest the use of 30%–50% Ge alloys to achieve absorption at the desired 1.3–1.5- μm wavelengths. However, a combination of materials and quantum mechanical considerations complicates matters. At Ge compositions of 30–50%, strained layer thickness cannot exceed 10–30 nm before the onset of misfit dislocations. Such dislocations would generate leakage currents that would be manifested as a dark current limit on photodetector sensitivity. The alloy layer may be stabilized by cladding it on both sides with Si layers and repeating the sequence in a superlattice to increase the total absorbing volume. The alloy then no longer behaves like the bulk material. The $\text{Si}/\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ forms a quantum well in which a trapped carrier cannot fall to the base energy level defined by the bulk strained alloy bandgap. Instead, each well has a series of bound quantum states and optical absorption occurs between the bound states in corresponding valence and conduction band wells. The net result of this so-called quantum size effect is that absorption occurs at wavelengths somewhat shorter than expected. Although quantum size effects make this application somewhat more difficult, in other instances they supply a valuable tool, as will be seen in discussions of intrasubband and tunneling devices.

The shift in wavelength from the bulk bandedges is apparent in Fig. 10 for *p-i-n* detectors consisting of *p*- and *n*-type Si layers on either side of an undoped 20-period superlattice [40]. For these measurements, unpatterned samples were cleaved and illuminated from the

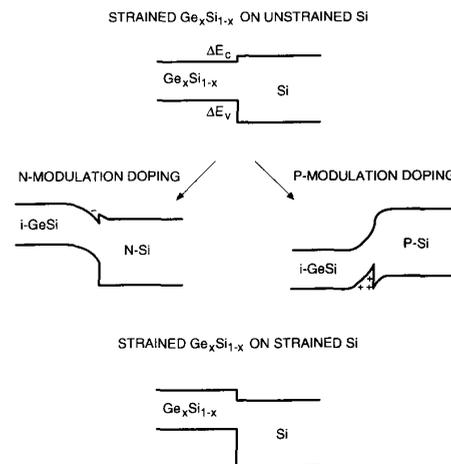


Fig. 8. Bandgap alignment for (100) $\text{Ge}_x\text{Si}_{1-x}$ and Si layers. Top, alignment for $\text{Ge}_x\text{Si}_{1-x}$ layers strained to match undistorted Si. Center, alignments for same strain configuration with selective doping of Si layer. Bottom, alternate band alignment achieved if $\text{Ge}_x\text{Si}_{1-x}$ and Si layers are grown on hypothetical $\text{Ge}_y\text{Si}_{1-y}$ substrate of intermediate composition such that alloy is under compression and Si under tension. Same effect is achieved if $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ is grown on very thick, relaxed $\text{Ge}_y\text{Si}_{1-y}$ buffer layer on top of Si substrate or if very thick superlattice is grown as in Fig. 7.

edge by unpolarized light from an optical fiber. This end illumination had the advantage of guiding the light within the superlattice by partial internal reflection and thereby increasing the absorption path. The coupling efficiency between the unlensed 5–8-mm diameter optical fiber and

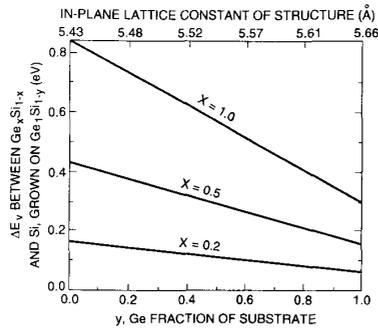


Fig. 9. Values of valence band discontinuities between strained $\text{Ge}_x\text{Si}_{1-x}$ and Si layers grown on unstrained $\text{Ge}_y\text{Si}_{1-y}$ buffer layers (with in-plane lattice constant indicated at top). Horizontal axis is substrate Ge fraction, y . Three curves are for strained $\text{Ge}_x\text{Si}_{1-x}$ /Si layers with Ge fractions, x , of 0.2, 0.5, and 1.0. Conventional growth of $\text{Ge}_x\text{Si}_{1-x}$ on Si represented by left axis indicating valence band discontinuity of 170 meV at alloy layer concentrations as low as 20%. Conduction band discontinuity can be calculated by subtracting valence band discontinuity from total bandgap difference indicated in Fig. 4.

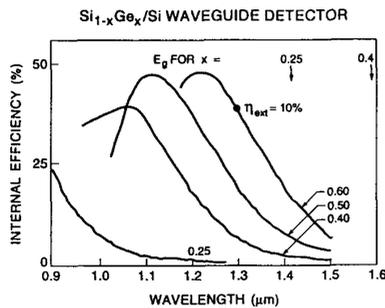


Fig. 10. Spectral response of p-i-n photodetector as a function of $\text{Ge}_x\text{Si}_{1-x}$ quantum well composition. p-i-n diode active regions consisted of a 20-period superlattice of $\text{Ge}_x\text{Si}_{1-x}$ wells clad by Si spacers. For Ge fractions of 0.25, 0.40, and 0.50, the wells were 75-Å wide with 250-Å spacers. For $x = 0.60$ the well was 60 Å and spacer 290 Å. Internal quantum efficiencies were based on conversion of external measurements including a 20% coupling efficiency of light from the fiber to superlattice. Arrows indicate wavelengths where room temperature absorption edges would begin in the absence of quantum size effects.

the 0.6- μm thick superlattice was estimated at 20%, leading to the indicated internal quantum efficiencies of up to 50%. The roll-off in absorption at short wavelengths is believed to occur because of a gradual loss in superlattice light guiding with a decrease in the alloy layer index of refraction. A subsequent modeling study [41] dealt with the tradeoffs in coupling efficiency, lightguiding, and absorption with possible changes in superlattice dimensions and periodicity. It concluded that the above structures came very near the optimum configuration for a simple p-i-n device.

Follow-on studies reported two improvements on the simple p-i-n device [42]–[44]. First, as shown in Fig. 11, silicon above the superlattice was patterned into a rib to provide lateral optical confinement that would supplement the vertical confinement of the $\text{Ge}_x\text{Si}_{1-x}$ layers. Second, the doping configuration was altered to provide for avalanche gain within the device. The avalanche mode

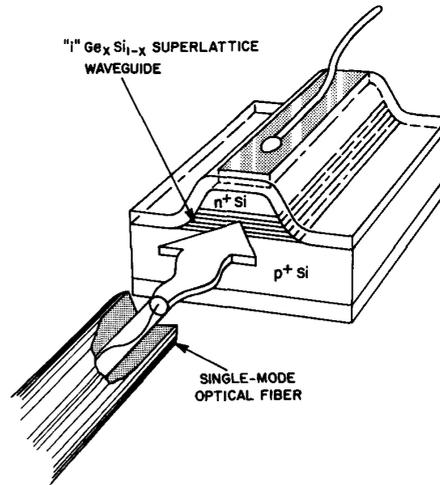


Fig. 11. Schematic cross section of rib-waveguide $\text{Ge}_x\text{Si}_{1-x}$ /Si photodetector. Structure of absorbing superlattice region is essentially the same as p-i-n diodes in Fig. 10 except that doping has been added to push high field avalanche region into Si layer adjacent to the superlattice.

takes advantage of one of the few points where silicon's electrical properties are superior to those of the typical III-V semiconductor: its electron multiplication coefficient is far larger than that of the hole. This translates into a noise advantage for the device if the doping is configured such that the high field avalanche region is contained entirely within the Si layers adjacent to the absorbing $\text{Ge}_x\text{Si}_{1-x}$ /Si superlattice [45]. With the combination of rib waveguiding and avalanche multiplication, internal gains of 12–17 were obtained, leading to a dc responsivity of 4 A/W and an external quantum efficiency of 400%. When the APD's were driven by light from a solid-state laser, pulsed response times were such that a 3-dB bandwidth of 8 GHz was achieved at a gain of 6. A pseudorandom bit stream transmitted at 800 MHz down a 45-km fiber produced bit error rates below the instrumental resolution of one part per billion.

In addition to fiber-optic detection, studies have explored the possible use of $\text{Ge}_x\text{Si}_{1-x}$ strained layers for detectors in the 7.5–15- μm range, which is of interest for applications as diverse as satellite resource mapping, night vision and medical thermography. Because imaging applications call for high resolution and thus for complex detector arrays, silicon would be a natural base material. These long wavelength devices tend to be based on the optical promotion of a hole from a doped $\text{Ge}_x\text{Si}_{1-x}$ layer into an adjacent Si layer. Because the transition involves only the valence bandedge, the devices are often referred to as intrasubband devices to contrast them with the intersubband (valence to conduction) devices discussed above.

In its simplest configuration [46], such a detector consisted of a single, relatively thick (40–400 nm) $\text{Ge}_x\text{Si}_{1-x}$ layer grown on a Si substrate. Both layers were p-type and

Ge fractions of 20%–40% were used. Absorption measurements at 4.4 K exhibited a broad tail falling between 2–10 μm with external quantum efficiencies from approximately 2%–0.8%. At 77 K, dark currents of 1 μA were noted at operating voltages. Very similar devices have been used in the recent, impressive, demonstration of a 400×400 pixel IR camera [47]. In this camera, the MBE $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ barrier regions were integrated directly on the CCD circuit, as shown in Fig. 12. When the circuit was driven by a 5-MHz clock at 53 K, a charge transfer efficiency of 0.999 per stage was achieved. Mounted in a camera, the device produced high resolution images out to 9.3 μm with good pixel to pixel uniformity and a minimum resolvable temperature of 0.2 K, as shown in Fig. 13. Individual $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ devices operated out to wavelengths of 16 μm at 30 K and, in even these early structures, exhibited higher quantum efficiencies than companion IrSi Schottky-barrier devices with similar cutoff wavelengths (i.e., peaks of 1.0% versus 0.8%).

B. Modulation-Doped Transistors

In the modulation-doped transistor, carriers are separated from their parent donor or acceptor atoms as they fall across a heterojunction to a lower energy undoped layer. If the carrier velocity is limited by electrostatic scattering with the dopant atoms, this separation will increase the carrier's mobility. The effect was first observed in the AlGaAs system [48] where it has now produced low temperature electron mobilities in excess of 10 million $\text{cm}^2/\text{V}\cdot\text{s}$ [49]. The earliest $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ modulation-doped mobilities were in the range of only several thousand $\text{cm}^2/\text{V}\cdot\text{s}$, but these structures were exploited in the first severe test of the ability of the strained layer alloy to withstand conventional device processing. Figure 14 shows the cross section of the planar p-channel device [50]. Significantly, the $\text{Ge}_{0.2}\text{Si}_{0.8}$ strained layers of this device were subjected to ion implantations and activation anneals, reactive ion etching and CVD oxide deposition. The transistor could be operated in both enhancement and depletion modes, and it yielded good transistor characteristics with room temperature transconductances of up to 3.2 mS/mm . An unimplanted, mesa etched n-type device also yielded good transistors with transconductances of up to 40 mS/mm [51].

Although devices survived conventional processing, they came nowhere near realizing the full potential of modulation doping. The mobility data for these early $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ layers are plotted at the bottom of Fig. 15. If modulation doping is fully exploited, the separation of carriers and ionized dopants should lead to transport comparable to that observed in very lightly doped layers. In the p-type device, the hole moves in a channel of $\text{Ge}_{0.2}\text{Si}_{0.8}$ and should have limiting mobilities somewhere between the low temperature hole values of $1 \times 10^4 \text{cm}^2/\text{V}\cdot\text{s}$ for Si [52] and $\sim 4 \times 10^4 \text{cm}^2/\text{V}\cdot\text{s}$ for Ge [53]. The measured peak was, instead, approximately 4000. In the n-type device, the channel is silicon and should thus have a mobility near Si's peak value of $10^5 \text{cm}^2/\text{V}\cdot\text{s}$, rather than the observed value of 1500.

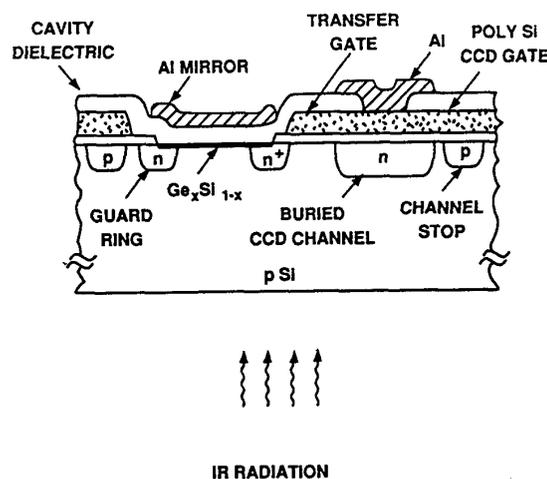


Fig. 12. Schematic cross section of $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ long wavelength infrared detector integrated directly with a CCD circuit and serving as one element in a 400×400 pixel camera array (by permission of B. Y. Tsaur [47]).

At the time, the discrepancy in p-type data was attributed to the likelihood of low level residual doping in the supposedly intrinsic $\text{Ge}_x\text{Si}_{1-x}$ channel, leading to latent ionized impurity scattering. Such a purely technological problem could have been corrected easily. Subsequent data make this explanation appear less likely. Experiments in many laboratories have not provided an improvement in p-type mobilities, including, most notably, experiments on layers grown by an entirely different CVD technique [54]. It now appears likely that mobilities are instead limited by scattering produced by the variation in atomic potential between the Ge and Si atoms of the channel. This idea is supported by recent data on a relaxed $\text{Ge}_x\text{Si}_{1-x}/\text{Ge}$ structure where the band alignment created a pure Ge hole channel. As shown by the single plotted point of Fig. 15, the mobility of this layer is significantly higher than that of $\text{Ge}_x\text{Si}_{1-x}$ at the same temperature (although it still falls short of the greater than 10^4 value of pure Ge at that temperature) [55]. If this explanation is correct, alloy scattering would place a fundamental, and rather modest, limit on the potential of p-type modulation doping in $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ heterostructures.

The limiting mobility of n-type modulation-doped layers has a clearer explanation and solution, but the practical potential is similarly clouded. It will be recalled that in the purely strain accommodated $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ heterostructure, only 20% of the net bandgap difference falls on the conduction bandedge, producing only very weak electron confinement. The n-type modulation-doped structures thus rely on the growth of thick or concentrated Ge layers to produce misfit dislocation accommodated relaxation as depicted in Figs. 2 and 7. The resultant strain produces strong electron confinement in the Si layers, but only at the cost of introducing threading dislocations through the



Fig. 13. Uncorrected infrared television images obtained with device of Fig. 12 (by permission of B.Y. Tsaur [47]).

device channel. The 10^9 – 10^{12} cm^2 threading dislocation densities of the earliest devices could easily account for the observed mobility degradation. As growth and annealing techniques have been developed for reducing these defect densities, reported electron mobilities have climbed steadily to recent reports of $10^5 \text{cm}^2/\text{V}\cdot\text{s}$ values in very thick, misfit accommodated layers. For the first time, these results are consistent with the level expected for the intrinsic channel material, and realize the full potential of modulation doping in silicon. Nevertheless, these samples have not yet been fabricated into devices and it is questionable whether the thick layers required for defect reduction ($\sim 5\mu\text{m}$) or the residual threading defect densities ($\sim 10^5/\text{cm}^2$) will ultimately be compatible with a commercial device.

C. Heterojunction Bipolar Transistors

In contrast to the somewhat uncertain modulation doping picture, heterojunction bipolar transistors (HBT's) appear to offer an ideal opportunity for the commercial application of $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$. The HBT [59], [60] provides an elegant solution to the conventional bipolar design problem: In the homojunction n-p-n transistor, the intended injection of electrons from emitter to base is compromised by the gain-degrading reverse injection of holes. Reverse injection cannot be avoided because electrons and holes face precisely the same emitter–base potential barrier and are governed by the same physics. The common alternative is to decrease the reservoir of available holes by decreasing the base doping. This increases the base resistance, forcing the use of wider bases, thereby placing an ultimate limit on operating frequency. Instead, the HBT uses an emitter material with a bandgap wider than that of the base and, for the n-p-n case, with the bandgap difference appearing primarily on the valence bandedge. The bandgap difference is thus manifested only as an increase in the injection barrier

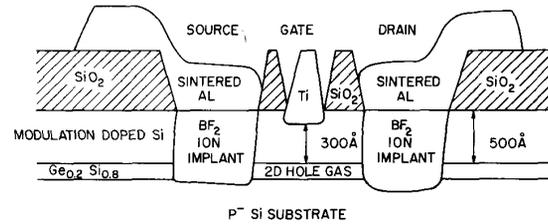


Fig. 14. Schematic cross section of a p-modulation-doped transistor fabricated using conventional silicon planar processing techniques.

for holes, largely removing constraints on base doping and thickness.

The desired band configuration, narrow bandgap base and large valence band discontinuity, is precisely that obtained with strain accommodated $\text{Ge}_x\text{Si}_{1-x}$ layers. Further, because the reverse injection of holes falls exponentially with barrier height, barrier enhancements as little as 60–120 meV suppress injection by factors of 10 and 100 at room temperature. Figures 4 and 9 show that such suppression is accomplished by the use of $\text{Ge}_x\text{Si}_{1-x}$ base layers with only 10–15% Ge. At conventional bipolar base thicknesses of less than 100 nm, such $\text{Ge}_x\text{Si}_{1-x}$ layers can be grown not only in the metastable strained mode but in the fully defect resistant equilibrium strained configuration of Fig. 6. Despite these favorable factors, the high speed HBT proved to be the most challenging test of this heterostructure materials system, its synthesis, and processing techniques.

The first reports of $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ HBT's appeared in the Fall of 1987 [61], [62] and Spring of 1988 [63]–[66]. The devices were all fabricated by MBE, as had been all of the initial material and device structures in this system. With one exception, these results were striking in their similarity: dc operation, current gains of 10–25 at room temperature, good but not ideal I–V and Gummel plots. The exception to this pattern [63] displayed a much higher gain of 250 but was notably an emitter down structure, where the emitter was fabricated not from an epitaxial layer but from the substrate Si. This pattern of rather modest results raised questions about the validity of the bandstructure data or the ultimate limits of the ultrahigh vacuum-based MBE synthesis technique. The latter suggestion gained support when, in 1989, the first high gain devices were fabricated by a competing 6 torr pressure, CVD-based technique.

The high gain results were obtained with a combination of the standard CVD and rapid thermal processing techniques [67]–[69]. In this hybrid, rapid thermal CVD (RTCVD) approach, lamp heating sources were energized intermittently to control layer thicknesses and customize layer deposition temperatures. With $\text{Ge}_x\text{Si}_{1-x}$ base layers of up to 31% Ge, this technique produced nearly ideal devices with gains of up to 325 in wholly epitaxial structures. These high gains were obtained despite the fact that base doping levels were estimated to be 50 times higher than that of the adjacent emitter regions. This apparent

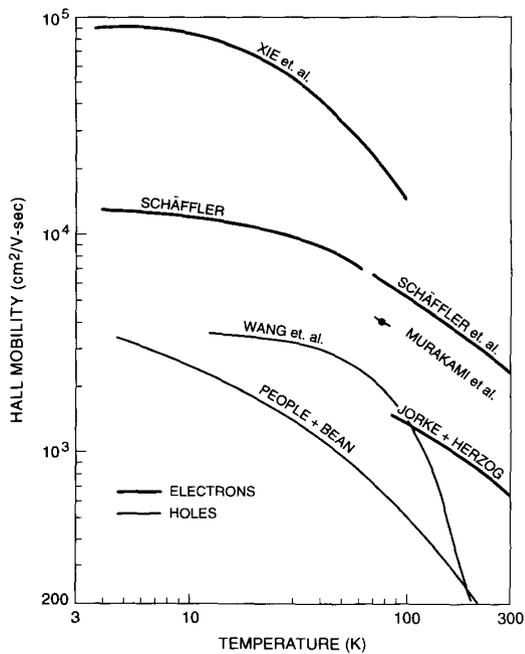


Fig. 15. Mobilities measured in modulation-doped $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ structures grown by various groups. Light lines are for holes in a $\text{Ge}_x\text{Si}_{1-x}$ channel clad by silicon. Point "Murakami" is for holes in a Ge channel clad by $\text{Ge}_x\text{Si}_{1-x}$. Heavy lines for electrons in structures grown on thick relaxed $\text{Ge}_y\text{Si}_{1-y}$ buffer layers to achieve strong electron confinement. (People and Bean [36], Jorke and Herzog [38], Wang *et al.* [54], Murakami [55], Schaffler *et al.* [56], Schaffler [57], Mii *et al.* [58]).

validation of the HBT concept was confirmed by control homojunction Si devices that exhibited gains 14 times lower than heterojunction devices. In Gummel plots of collector and base currents, the HBT devices exhibited ideality factors of $n = 1.03$ over six decades of current. In later, 23% Ge base devices, ideality factors of 1.01 were achieved.

In the initial RTCVD structures, relatively crude (e.g., $30\mu\text{m} \times 30\mu\text{m}$) structures were employed, limiting AC performance. This was addressed in follow-on experiments where direct-write electron beam lithography was employed to write features as small as 500 nm [70]. In a series of mesa devices, HBT's were fabricated with base doping varying from 7×10^{18} to $1 \times 10^{20}/\text{cm}^3$ and base widths from 15 to 25 nm. The resultant gains ranged from 32 to 48 and compared with values of 0.2 that would have been expected in the absence of heterojunction action. For a device with dual $1\mu\text{m} \times 10\mu\text{m}$ emitter stripes, a unity gain cutoff frequency, f_t , of 28 GHz was measured. This compared quite favorably with an estimated f_t of 33 GHz calculated for an idealized transistor of this device's dimensions and compositions.

The strong RTCVD results appeared to confirm doubts about the MBE growth technique. Although this issue might appear to be of interest only to those in the crystal growth area, it has broader ramifications. It is no simple

problem to synthesize semiconductor layers only a small number of atomic layers thick. In this system, only MBE has consistently demonstrated the 0.1–5-nm layer control necessary to reproducibly fabricate the quantum well devices discussed elsewhere in this review. Further, even in HBT structures where minimum layer thicknesses fall in the "thick" 10–50 nm range, those involved in the successful RTCVD effort conceded that layer control was still an issue [71]. Substantial effort is being directed toward enhancing the control of CVD-based GeSi growth. However, most approaches involve reduced pressure growth and ultrahigh vacuum pumping techniques [72]–[75], and early commercial implementations employ stainless steel chamber fabrication¹. Questions (and concerns) about UHV schemes and materials are thus of generic interest.

Eventually, it was demonstrated that doubts about MBE and vacuum processing were grounded but correctable. Limitations in MBE device performance were shown to be due to trace metal contamination from components in the vacuum system [76]. This contamination was especially pernicious in that concentrations on the order of 1 part per billion can begin to degrade the performance of a sensitive minority carrier device such as the HBT. With changes in substrate heating materials and procedures, we have now been able to obtain MBE-based HBT's with routine gains in excess of 2000 and cutoff frequencies in the same 20-GHz range achieved in RTCVD structures processed side by side [77]. These results bode well for $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ structures that, whatever the ultimate synthesis technique, will inevitably rely on a large component of high vacuum processing to achieve requisite control.

It is in another area of control, that of lateral device processing, where improvements have lead to the most spectacular $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ bipolar transistor results. In the device of Figs. 16 and 17, a polycrystalline emitter is deposited through a window on a $\text{Ge}_x\text{Si}_{1-x}$ base that, in turn, partially overlies an oxide window to an epitaxial collector [78]. Conventional CVD techniques are used for the emitter and collector, but for the base layer a variant of CVD was used that employs ultrahigh vacuum practices to largely eliminate residual gases and thereby reduce growth temperatures. The important feature is that, for both of the necessarily large emitter and base contact areas, most or all of the semiconductor overlies a dielectric rather than another semiconductor layer. This use of dielectric overgrowth eliminates large junction areas that serve no positive device function but whose charging would severely limit device speed. Rigorously speaking, this device is not a HBT in the sense that it was originally proposed. The Ge concentration of the base falls to zero at the emitter–base junction and electrons and holes face the same injection barrier. The Ge profile is instead employed to create a bandgap tapering gradually toward the collector. Because the valence bandedge in the p-type base is pinned near the Fermi level, this taper is manifested as a slope in the conduction bandedge. The slope is equivalent to a

¹See, for example, the cluster tool based designs of Rapro Inc.

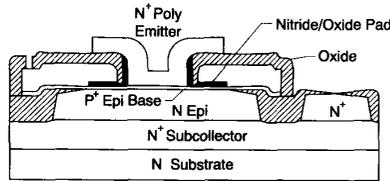


Fig. 16. Schematic cross section of $\text{Ge}_x\text{Si}_{1-x}$ graded base bipolar transistor. Note that emitter and base contacts largely overlie dielectric layers rather than deeper semiconductor junctions thereby reducing parasitic capacitances (by permission of G. L. Patton [67]).

surprisingly large field of about 20 kV/cm that serves to sweep the injected electrons rapidly through the base.

The resulting device exhibits a classic 20-dB/decade roll-off in gain that extrapolates to a unity gain cutoff frequency of 75 GHz. This cutoff is an all time record for a silicon-based transistor. The calculated cutoff is 79 GHz, and the agreement leads to the estimate of a total device transit time of 1.9 ps, divided 0.35, 0.75, and 0.6 ps between emitter, base and collector layers respectively. In subsequent ECL circuits based on a self-aligned refinement of these devices, ring oscillators yielded devices with switching times as small as 28.1 ps for operating temperatures ranging from room temperature to liquid nitrogen temperature [79]. In these devices, the peak Ge base concentration of 8% is well under the equilibrium strain limit and should thus be fully resistant to normal integrated circuit processing procedures.

D. The Exotic Devices: Tunnel Diodes, NERFET's, and LED's(?)

The above devices are among the best known heterostructure designs and are also those for which we have fairly complete results in the $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ materials system. We turn now to a smaller, more conjectural, body of work that may nevertheless point the way to future device configurations.

In the AlGaAs system, quantum wells have been used to fabricate a new class of devices based on the resonant tunneling effect [80]–[83]. In their I–V characteristics, these devices display negative resistance regions that could be useful in oscillators and a periodic conduction that has been proposed as the basis for a possible multivalued (nonbinary) logic circuit design [84]. The schematic of a $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ resonant tunneling structure is shown in Fig. 18. At appropriate bias, holes should be able to tunnel from a $\text{Ge}_x\text{Si}_{1-x}$ cladding layer through one of several bound states in the center alloy quantum well to the other cladding layer. This tunneling is demonstrated in the low temperature I–V characteristic of Fig. 19 [85]. A first weak tunneling feature is apparent at 0.4 V and a second stronger feature at 0.7 V. At biases immediately above each tunneling feature, the bound state rises above the valence band edge of the cladding layer and conduction falls. For the second state, this produces a negative differential feature with a 2.1:1 peak-to-valley ratio at 4.2 K. As would be expected for this

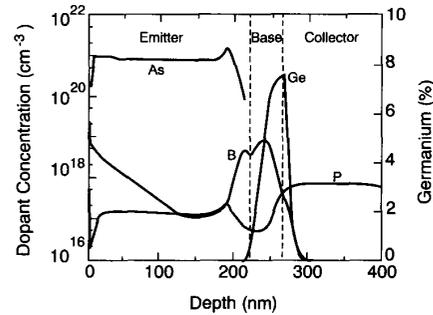


Fig. 17. Concentration profiles of device of Fig. 16 showing doping and grading of Ge from 0 to 8% across base layer (by permission of G. L. Patton [67]).

symmetric structure, mirror image features are observed at negative biases.

Follow-on experiments [86]–[89] yielded fundamentally similar I–V results although considerable additional effort was put into identifying the precise quantum well levels responsible for the transitions. One $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ paper reported transistor results but did not include data showing a peak in collector current versus emitter–base bias (i.e., negative transconductance) [90]. Such data would confirm resonant tunneling transistor action. As a whole, these $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ results are not yet up to the standards of the AlGaAs system where peak-to-valley ratios of 30:1 have been achieved, series of up to 16 peaks observed, and clear transistor action demonstrated. In part the differences may be due to the rather complex, strain split quantum well structure of the $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ system that will produce close and possibly overlapping bound states. However, there is almost certainly a large learning curve component where, for instance, materials improvements derived from HBT experience have not yet been fully applied. As experience grows, improved results will give a better picture as to the potential of resonant tunneling in this system.

Another negative resistance device has been reported based on the emission of hot carriers from a $\text{Ge}_x\text{Si}_{1-x}$ channel. This so-called negative resistance field effect transistor (NERFET) combines an FET with a floating buried gate (see Fig. 20) [91]. Holes are conducted along a p- $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ channel covered on the surface side by an intrinsic Si layer. The channel provides a connection between implanted source and drain regions in an FET-like device. Below the channel is an n-p-n sandwich of silicon layers. At low source–drain biases, conduction increases normally until carriers become energetic enough that they begin climb over the barrier to the adjacent n-Si and fall into the floating p-type Si layer. This floating layer charges up tending to deplete the $\text{Ge}_x\text{Si}_{1-x}$ channel. Depletion produces a 2:1 negative differential resistance in the 77 K source–drain current. Application of a substrate bias shifts the onset of negative differential resistance. Because this negative resistance depends upon the charging of a floating layer, the device would be suitable for memory rather than

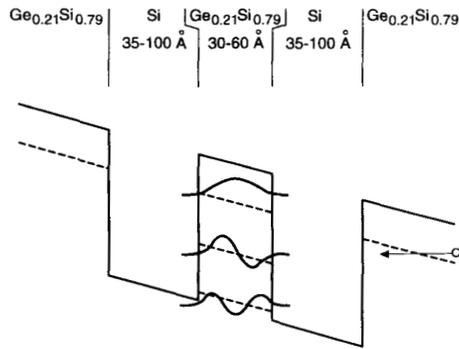


Fig. 18. Schematic of $\text{Ge}_x\text{Si}_{1-x}/\text{Si}/\text{Ge}_x\text{Si}_{1-x}/\text{Si}/\text{Ge}_x\text{Si}_{1-x}$ valence band configuration in a resonant tunneling diode. At appropriate biases, the Fermi level of holes in the right alloy layer will match up to one of the multiple bound energy levels in the center alloy quantum level. At those biases, holes can tunnel entirely through the structure. Serpentine lines in center layer denote the form of the bound hole wavefunction.

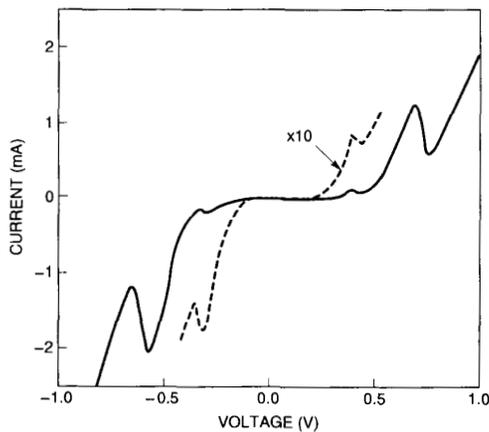
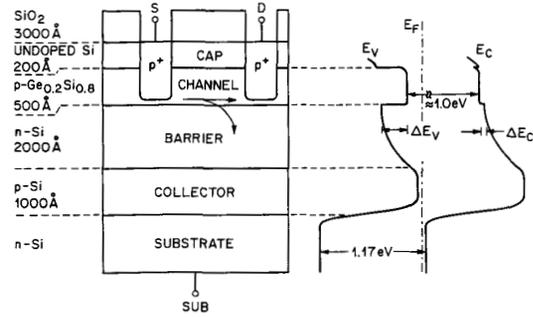


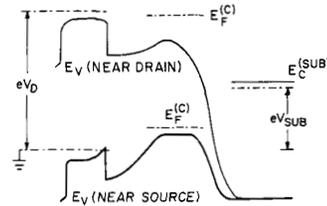
Fig. 19. A 4.2 K I-V characteristic of resonant tunneling diode shown in Fig. 18. Tunneling through lowest bound state indicated by small peak at ± 0.35 V. Strong tunneling through second bound state at ± 0.7 V is followed by negative differential roll-off with peak to valley ratio of 2.1:1 (by permission of D. C. Houghton [85]).

logic applications. The device illustrates the diverse ways in which Si-based heterojunctions might be employed, but much work remains to be done before the full potential can be assessed.

This brings us to a final, most intriguing, and ultimately elusive possibility for the $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ system—that of a Si-based light-emitting diode (LED). The bandstructure of a conventional semiconductor is derived from the basic atomic periodicity of the crystal lattice. In Si or Si-rich $\text{Ge}_x\text{Si}_{1-x}$, this periodicity leads to an indirect bandgap with the valence band maximum at $k = 0$ and multiple conduction band minima near the boundary of the Brillouin zone in the six equivalent $\{100\}$ directions (as illustrated by the solid heavy lines in Fig. 21). Because of this indirect bandgap, electrons and holes can recombine only with the



(a)



(b)

Fig. 20. Cross section and equilibrium band diagram for NER-FET device illustrating normal flow through $\text{Ge}_x\text{Si}_{1-x}$ channel and real space transfer of hot holes to floating p-Si layer.

help of a third, momentum-conserving phonon in what is then a slow and improbable process. Light emission from Si is thus very weak and is usually compromised by nonradiative recombination via trace metal contaminants.

In a heterostructure system, one can introduce another fundamental periodicity with the growth of a superlattice. As the period of this superlattice approaches that of the base semiconductor, the Brillouin zone will be folded upon itself. In a Si-based material, it was expected that certain indirect conduction band minima might be folded back toward $k = 0$, producing a direct or near-direct bandgap. Structures, such as that of Fig. 5, were grown to explore this possibility. Early work on such atomic layer superlattices (i.e., with periodicities from 2 to 10 atomic layers) showed signs of such a zone-folding effect in the appearance of new transitions measured by the electroreflectance technique [92], [93]. However, when such samples were illuminated by light or driven as diodes, they produced no signs of enhanced light emission.

These structures were examined theoretically, and it was argued that sufficient account had not been taken of the importance of strain [94]. In a cubic Si-like lattice, the six conduction band minima lie in pairs along the three orthogonal $[100]$, $[010]$, and $[001]$ directions and are equivalent in energy. In a strained layer superlattice, the sixfold degeneracy will be split by the compression in the growth plane and dilation perpendicular to it. As shown by the lighter solid lines of Fig. 21, the orbitals corresponding to the superlattice direction are split to a higher energy. These two orbitals may then fold toward

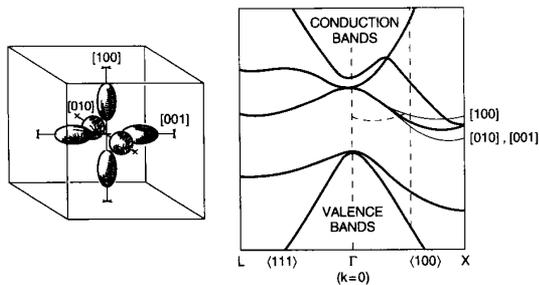


Fig. 21. Left: Schematic representation of normal, equivalent, conduction band orbitals. Right: Bandstructure for Si or dilute $\text{Ge}_x\text{Si}_{1-x}$ alloy. Vertical axis is energy, horizontal axis is electron or hole momentum in $\langle 111 \rangle$ and $\langle 100 \rangle$ k -space directions. Lighter solid lines represent strain splitting of conduction band that would be produced by growth of $\text{Ge}_x\text{Si}_{1-x}$ on $\langle 100 \rangle$ Si. Curved dashed line indicates the folding of the $[100]$ split band that would occur for a superlattice grown on a $\langle 100 \rangle$ surface with a periodicity twice that of the silicon crystal cell (and therefore with a Brillouin zone $1/2$ as wide). Such folding can produce a near direct bandgap, but minimum conduction band state is still indirect at the other strain split and unfolded orbitals. (Note in the figure and text: $[\]$ brackets denote a specific direction; $\langle \ \rangle$ represent a family of equivalent directions such as $[100]$, $[010]$, and $[001]$; $\{ \}$ denote a specific plane; and $\{ \}$ a family of equivalent planes).

the $k = 0$ zone center as shown by the dashed line. Unfortunately, the remaining four unfolded orbitals still lie at a lower energy and provide a minimum electron state that is still indirect and, therefore, largely non-luminescent! As might be guessed, the splitting of the orbitals will change as a function of strain and growth orientation. In a superlattice grown on a $\{110\}$ surface, direct bandgap folding should occur but selection rules still disallow efficient electron-hole recombination. In a symmetrically strained, misfit accommodated $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ superlattice, folding is thought to occur without a selection rule prohibition. This possibility has been tested and there are signs of weak photoluminescence [95]. However, as noted before, this symmetric strain configuration is produced only at the expense of high threading dislocation densities that not only lead to confusion as to the source of the light but, based on III-V semiconductor experience, would appear to be incompatible with a long-lived optical device. Most recently, for certain experimental structures, additional questions have been raised as to whether observed signals are correctly attributed to the monolayer superlattices or might instead come from Ge or Si spacer layers [96].

VII. SUMMARY AND CONCLUSIONS

The semiconductor heterostructure greatly enhances the range of device configurations and can offer access to entirely new physical concepts such as tunneling, quantum size, and hot carrier effects. Heterostructural pairings come quite naturally to the compound semiconductors where there are direct structural and chemical matches, such as AlAs to GaAs or possible alloy couplings, such as $\text{Ga}_{0.47}\text{In}_{0.53}\text{As}$ to InP. In contrast, there is no natural semiconductor partner for silicon. Certain column III-V materials have both the appropriate lattice structure and spacing

but are composed of materials that dope silicon. Lattice mismatched pairings necessarily lead not only to high dislocation densities at the heterojunction but to dislocations that thread through the entire overgrown layer structure. Dissimilar pairings of any kind are prone to severe problems of layer morphology and discontinuous growth. The one alternative, a strained epitaxial match with a chemically compatible semiconductor, such as Ge, appeared to be fundamentally limited by both layer thicknesses and the rather small decrease in $\text{Ge}_x\text{Si}_{1-x}$ bandgap.

Several findings have changed this view. Investigations showed that newer epitaxial growth techniques can synthesize smooth, continuous layers of $\text{Ge}_x\text{Si}_{1-x}$ on Si for all compositions, down to layer thicknesses of atomic monolayer dimensions. Second, the strained layer pairing of $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ turned out to be considerably more robust than expected. Although strain seemed to imply instability, in a crystalline structure its relief requires the formation of misbonded dislocation atom rows that can represent a much higher energy state. Thin or dilute $\text{Ge}_x\text{Si}_{1-x}$ layers are thus entirely stable, and much thicker or concentrated layers can be grown in a metastable form that is quite resistant to dislocation formation. Finally, strain causes a pronounced narrowing of the $\text{Ge}_x\text{Si}_{1-x}$ bandgap, and dilute layers are sufficient to produce strong bandedge discontinuities with silicon.

The $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ strained layer bandstructure yields much larger barriers in the valence than in the conduction band, and it thus most effective at the manipulation of holes. It is therefore natural for application to the n-p-n heterojunction bipolar transistor where dilute, fully stable, strained layers have yielded pronounced improvements in device performance and graded base bipolar transistors have achieved new speed records for silicon-based devices. More concentrated layers have been applied to a variety of devices including high performance optical fiber detectors, and exploratory modulation-doped transistors, far infrared detectors, tunneling, and real space carrier transfer devices.

The strong manipulation of electrons is possible but more difficult. Pronounced conduction band differences can be achieved only if both $\text{Ge}_x\text{Si}_{1-x}$ and Si are strained. This configuration would occur naturally if a layered structure were grown on a $\text{Ge}_y\text{Si}_{1-y}$ alloy substrate of intermediate composition. However, on the technologically relevant Si substrate it is achieved only if a thick, lattice mismatched, alloy buffer layer is first grown. The buffer layer necessarily has a dense array of dislocations at the Si interface, and in all experiments to date, a large number of these dislocations bend up to propagate through the epitaxial structure, clouding device prospects. Nevertheless, progress has been made, and most notably, near ideal electron mobilities have recently been achieved in modulation-doped structures, despite dislocations.

It had been hoped that bandstructure manipulation might also yield the Holy Grail of silicon materials research: a light source. While superlattices do produce fundamental alterations in bandstructure, a $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ light source does not appear to be on the horizon, at least not in a practical

configuration. The demonstrated heterostructure capabilities do, however, add a rich new texture to the silicon landscape. And we have only begun to explore the possibilities that transform this most mature of semiconductors into the newest heterostructure material.

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